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300 Series Beta Computers

Field Service Manual

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Compucorp[®]

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The CompuCorp Beta Computer combines, for the first time, sophisticated system technology with the portability of a hand-held computer. Section I describes the special features, functional organization, and specifications of the Beta Computer.



Figure 1-1 Typical Beta Computer

1.1 BETA COMPUTER SPECIAL FEATURES

The Beta computer features a signed 13-digit mantissa with a signed 2-digit exponent and 12 data storage registers capable of performing full register arithmetic. Also featured is a program memory of 160 program steps.

The Beta Computer is full compatible with the 392 Cassette Drive and the 395 Teleprinter Interface, allowing data exchange between the computer memory and the peripheral devices.

1.1.1 STANDARD BETA COMPUTER FUNCTIONS

The Beta Computer performs standard algebraic and arithmetic functions, including raising any number to any power-of-ten. The standard computer functions are described below while the special functions of the Beta 326 Scientist Computer are described in Par. 1.1.2. The computer can:

- a. Perform algebraic arithmetic. The keys +, -, X and ÷ can perform a series of algebraic operations without requiring intermediate results
- b. Perform bracket operations. The two parentheses keys allow direct computation of formulae without separately calculating the value within the parentheses. When parentheses are opened, the nesting level (1, 2, 3, or 4) is displayed by the leftmost digit of the display
- c. Raise numbers to a power. The base and exponent may be integral or fractional, positive or negative; however, raising a negative number to a noninteger power causes error
- d. Perform full register arithmetic. Addition, subtraction, multiplication, and division may be performed into or out of any data register
- e. Calculate the square and square root of the value in the Entry Register
- f. Compute the reciprocal of the number in the Entry Register, or compute the factorial of a non-negative integer in the Entry Register up to 69
- g. Compute the common and natural logarithms and anti-logarithms of the number in the Entry Register
- h. Perform both conditional and unconditional branches and jumps from when operating from program control
- i. Receive data from or transmit data to an external peripheral device.

1.1.2 BETA SCIENTIFIC FUNCTIONS

Aside from the functions described in Par. 1.1.1, the 326 Scientist performs a variety of special functions. The 326 Scientist can:

- a. Compute the sine and arcsine of the angle in the Entry Register
- b. Compute the cosine and arccosine of the angle in the Entry Register
- c. Compute the tangent and arctangent of the angle in the Entry Register

- d. Convert Cartesian coordinates (X, Y) to polar coordinates (θ , r) and polar coordinates to Cartesian coordinates
- e. Compute trigonometric functions in either grads or degrees, as determined by the GRAD/DEG switch
- f. Convert radians to degrees or grads, and degrees or grads to radians, as determined by the GRAD/DEG switch
- g. Insert the value of π or 'e' into the Entry Register
- h. Convert English units of measurement to Metric units, and Metric units to English units
- i. Convert UK gallons to liters, and liters to UK gallons
- j. Convert decimal degrees to degrees/minutes/seconds, and degrees/minutes/seconds to decimal degrees
- k. Compute the standard deviation and mean for both grouped and ungrouped data
- l. Compute the absolute value of the number in the Entry Register.

1.2 FUNCTIONAL DESCRIPTION

The computer contains the seven major assemblies illustrated in Fig. 1-2. Figure 1-3 is a functional block diagram of the computer.

Because of its high versatility and high packing density, MOS/LSI (Metal Oxide Semiconductor/ Large Scale Integration) logic arrays form the basic building blocks of the computer. MOS/LSI logic is contained in chips soldered to the printed circuit board. The detailed description in Section II includes a description of each chip at the block diagram level.

1.2.1 VOLTAGE ADAPTER

The voltage adapter is physically separate from the computer. The AC adapter converts the AC supply (117/220/240 volts, 48-62 Hz) to a DC supply for the computer.

1.2.2 POWER SYSTEM

The power system, including the Converter board, power distribution assembly and batteries, generates the voltages required by the computer. The Converter board also contains the

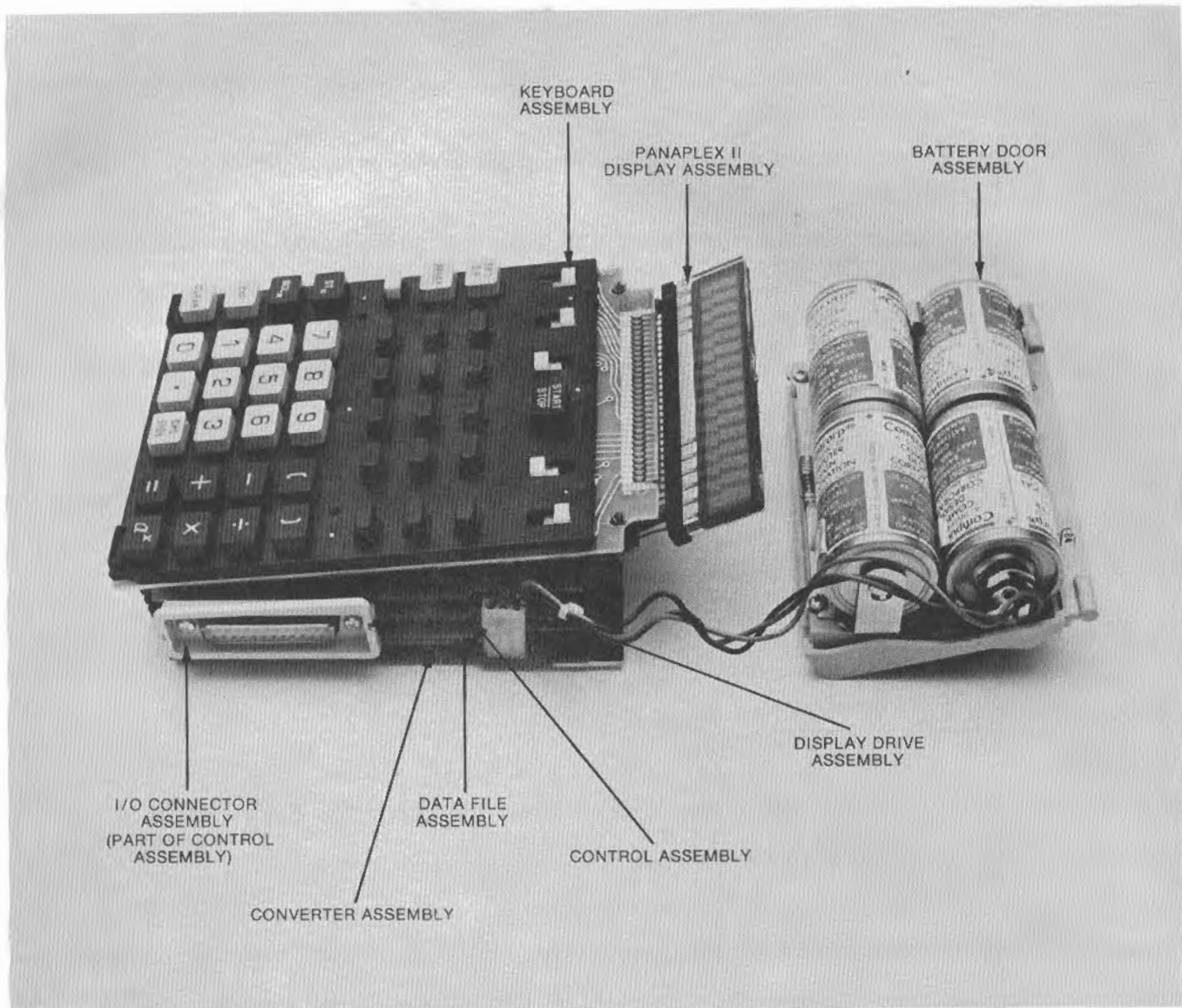


Fig. 1-2 Major Assemblies

clock circuits to supply clocks $\Phi 1$ and $\Phi 2$ to all circuit boards, and ΦR to the Data File. In addition, it generates the low battery detector signal, $\overline{INL2}$.

1.2.3 DISPLAY DRIVE

The Display Drive assembly is the printed circuit board located directly beneath the keyboard assembly. The Display Drive assembly performs three functions: encode key depressions, decode display output signals, and receive status information and data from peripheral devices.

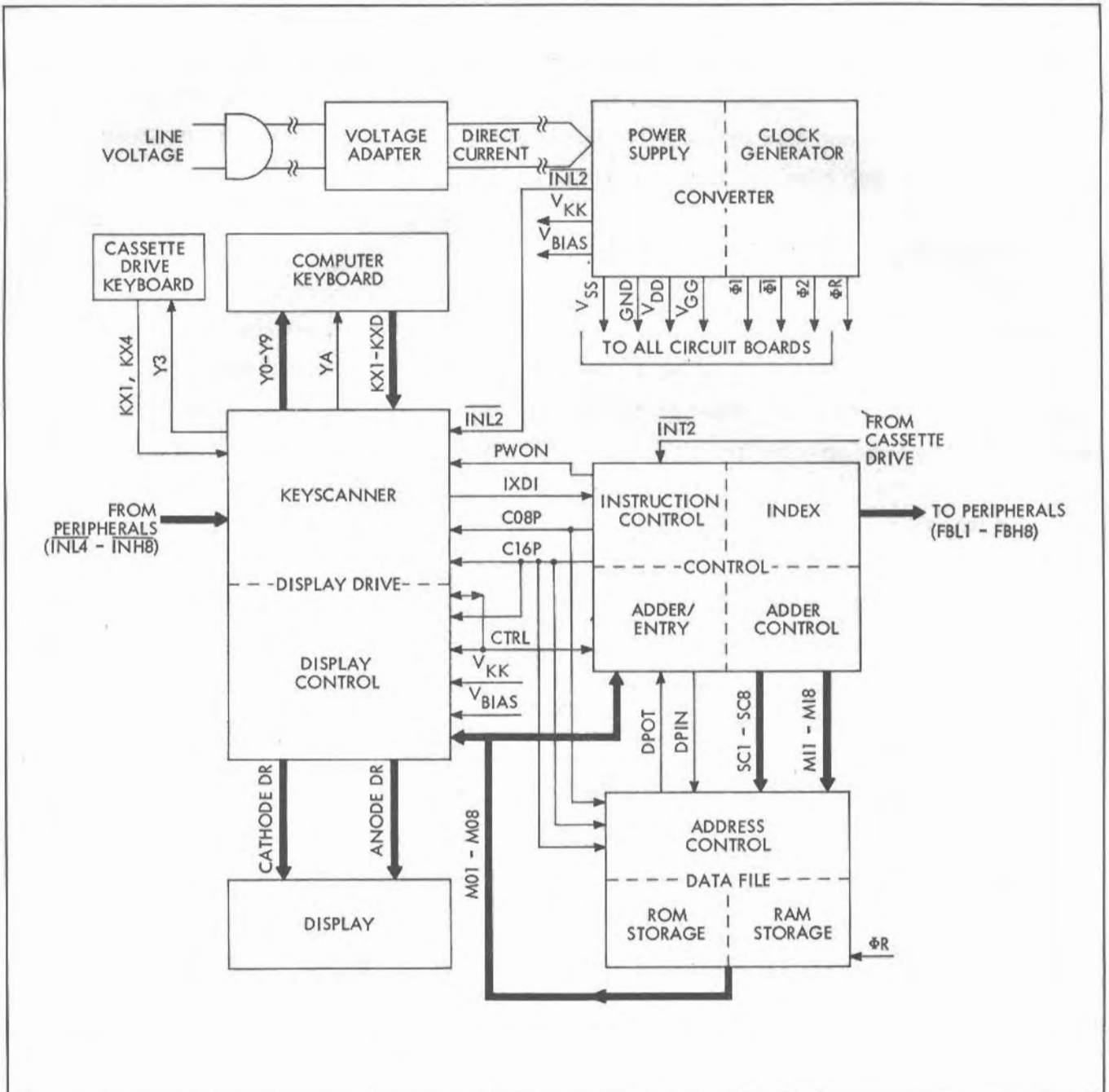


Fig. 1-3 Functional Block Diagram

The keyscanning circuits continually test the condition of the switches on the keyboard and the Display Drive board. The keyscanner translates the detection of a closed switch into a binary-coded-octal number and transmits it to the Control assembly via line IXDI.

Status information and data from peripherals is read by the keyscanner chip on the Display Drive board. The ROM peripheral control micro-program determines the intervals at which device status and data are read.

The Display Drive board contains the display control circuits. The Data File output is converted into a usable format by the display control circuits as directed by the Control assembly. This operation includes aligning the number in accordance with the decimal point setting, converting numerical information into segment selection signals, enabling the display anodes at the proper digit time, and blanking unused digits.

1.2.4 KEYBOARD

Physically the keyboard consists of 43 momentary-action pushbutton switches and five slide switches. These switches complete the signal path for the keyscanner signals Y0 through Y9, and YA. The scanning pulses return to the keyboard on 14 keyboard return lines (K-lines). The switches are mounted on a printed circuit board which is part of the keyboard.

1.2.5 DISPLAY

The display is a 16-digit, cold cathode glow discharge panel. It operates in a multiplexed mode wherein like cathode segments are bussed together and are time shared among all digit positions. The anodes of the 16-digit positions are enabled sequentially, causing those cathode segments which are enabled to turn on.

1.2.6 CONTROL

The Control assembly is a printed circuit board with four MOS/LSI chips. The Control assembly contains the Entry Register, an Index Register, and two flag registers. It also contains the Adder logic for performing logic operations on the Index Register. The Control Assembly generates five timing signals, CO1P, CO2P, CO4P, CO8P, and C16P, which define bit times within a 20-bit machine cycle. An Instruction Generator translates microinstructions from the ROMs into control signals for the combinational logic chips. These control signals are transferred serially via CTRL.

Control also updates data and program address stores as required. New address information from the Control is transferred serially to the Data File via DPIN. Address stores from the Data File transfer serially to Control via DPOT. The Control also transfers information from the

program address pointer to the Data File along four parallel lines: SC1, SC2, SC4, and SC8. The Control generates a power-on signal (PWON) which clears user memory and establishes initial logic conditions when the computer is first turned on. The Data File input lines: MI1, MI2, MI4, and MI8 originate on the Control Board.

The Control Assembly also regulates peripheral equipment operations by software manipulation of Flag Group B. The software manipulation is accomplished by permanently stored microprograms within a ROM.

1.2.7 DATA FILE

The Data File is a printed circuit board which uses read-only-memories (ROMs) and random-access-memories (RAMs). The ROMs contain permanently stored micro-programs while the RAMs provide storage for user data and program, and working storage for calculations performed by ROM micro-programs. The Data File contains a combinational logic chip which receives control instructions and address information from the Control Assembly. It converts these inputs into a RAM enabling signal, a write enable signal, and fifteen address signals.

The ROMs contain the micro-instructions to perform the operation indicated by a keyboard key depression or user program instructions.

1.3 SPECIFICATIONS AND LEADING PARTICULARS

Table 1-1 lists the specifications and leading particulars for the Beta computer.

Table 1-1
SPECIFICATIONS AND LEADING PARTICULARS

Characteristic	Specification	
	Computer	Voltage Adapter
Power Requirements		
Voltage	5.5-7 .0VDC	117VAC/220VAC/240VAC
Power	11W	
Battery		
Life	3.5 Hours without charging	N/A
Charging Rate	400ma (max)	N/A
Current Capacity	N/A	1.5 amperes @ 5.5VDC (min)
Environment (Operating)		
Temperature	-6.7°C to 40.6°C	-6.7°C to 40.6°C
Humidity	0 to 95 percent (noncondensating)	0 to 95 percent (noncondensating)
Dimensions and Weights		
Width	5 inches (12.70cm)	2.5 inches (6.34cm)
Depth	2 inches (5.08cm)	2.5 inches (6.34cm)
Length	9 inches (22.86cm)	6 inches (15.24cm)
Weight	3.5 pounds (1.6kg)	2.4 pounds (1.1kg)
Logic Levels		
Logic 1	V _{SS}	N/A
Logic 0	GND	N/A
Number Capacity		
Display	16 characters	N/A
Internal		
Mantissa	Sign plus 13 digits	N/A
Exponent	Sign plus 2 digits	N/A
Storage Capacity		
Data	Twelve 64-bit registers	N/A
Program	160 steps	N/A

Section II PRINCIPLES OF OPERATION

Section II describes computer operation at the chip and component level. The purpose of the section is to provide the field service representative with sufficient knowledge of the internal organization and operation of the computer to perform maintenance with a minimum of time and effort.

2.1 VOLTAGE ADAPTER PRINCIPLES OF OPERATION

The AC adapter converts the AC supply to a direct-current output to operate the computer and recharge the batteries. The schematic diagram Fig. 2-1 shows the 117/220/240 VAC adapter.

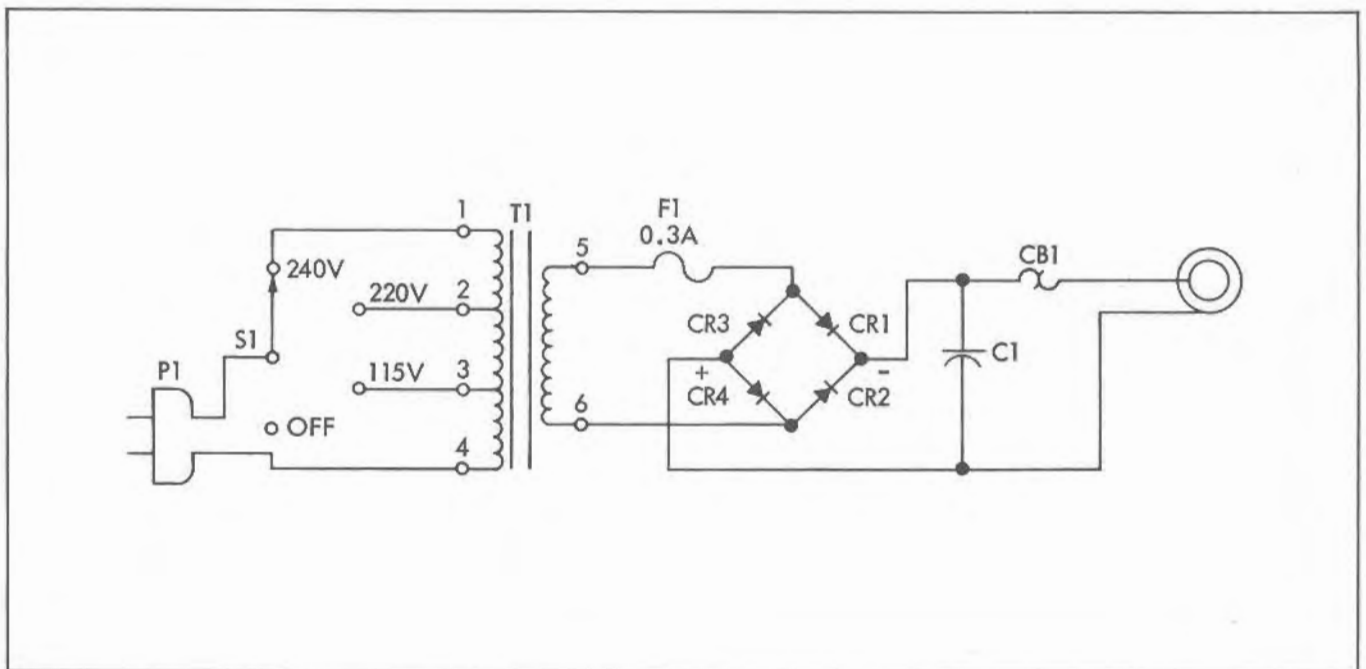


Fig. 2-1 AC Adapter, Schematic Diagram

The AC input passes through adapter switch S1 to the transformer. The rotary switch changes the primary connections to allow operation from either 117, 220, or 240 volts. The primary windings are in series for all voltages.

The stepped-down secondary voltage passes through fuse F1, and is rectified by a bridge rectifier comprised of CR1 - CR4. C1 filters the DC ripple voltage. The DC voltage passes through

thermal switch CB1 to output plug P2. The adapter output is approximately 6 volts at 1.4 amperes under load and approximately 12 volts open circuit.

2.2 POWER SYSTEM PRINCIPLES OF OPERATION

The power system consists of four batteries, a power distribution assembly and a Converter printed circuit board. The batteries and the power distribution assembly are located in the battery compartment. These components supply power from the batteries or voltage adapter to the Converter printed circuit board.

The batteries are rechargeable nickle-cadmium cells with a rated output of 1.25 volts at 1 ampere. Depending upon the vendor, the capacity is 3 to 4 ampere-hours and the life expectancy about 1000 charge-discharge cycles. All batteries approved for use in the computer contain a pressure vent.

2.2.1 POWER DISTRIBUTION ASSEMBLY

Figure 2-2 is the schematic diagram of the power distribution assembly. When the computer operates on batteries, the negative pole of cell BT4 is Connected to BAT CHGR through connector JC1. BAT+ connects to the positive pole of BT1 through ON-OFF switch S1.

With the voltage adapter installed, the contact between terminals 2 and 3 of JC1 is open, and the negative side of the adapter output goes to the Converter board via the BAT CHGR line. The positive adapter output goes to BAT+. BAT- applies the charging current from the Converter board to the batteries.

2.2.2 BATTERY CHARGING CIRCUITS

Refer to Fig. 2-2 for the following discussion.

Transistors Q1, Q2, and Q3 regulate the battery charging current. With the computer connected to an operating voltage adapter, the charging current flows from BAT CHGR, through the

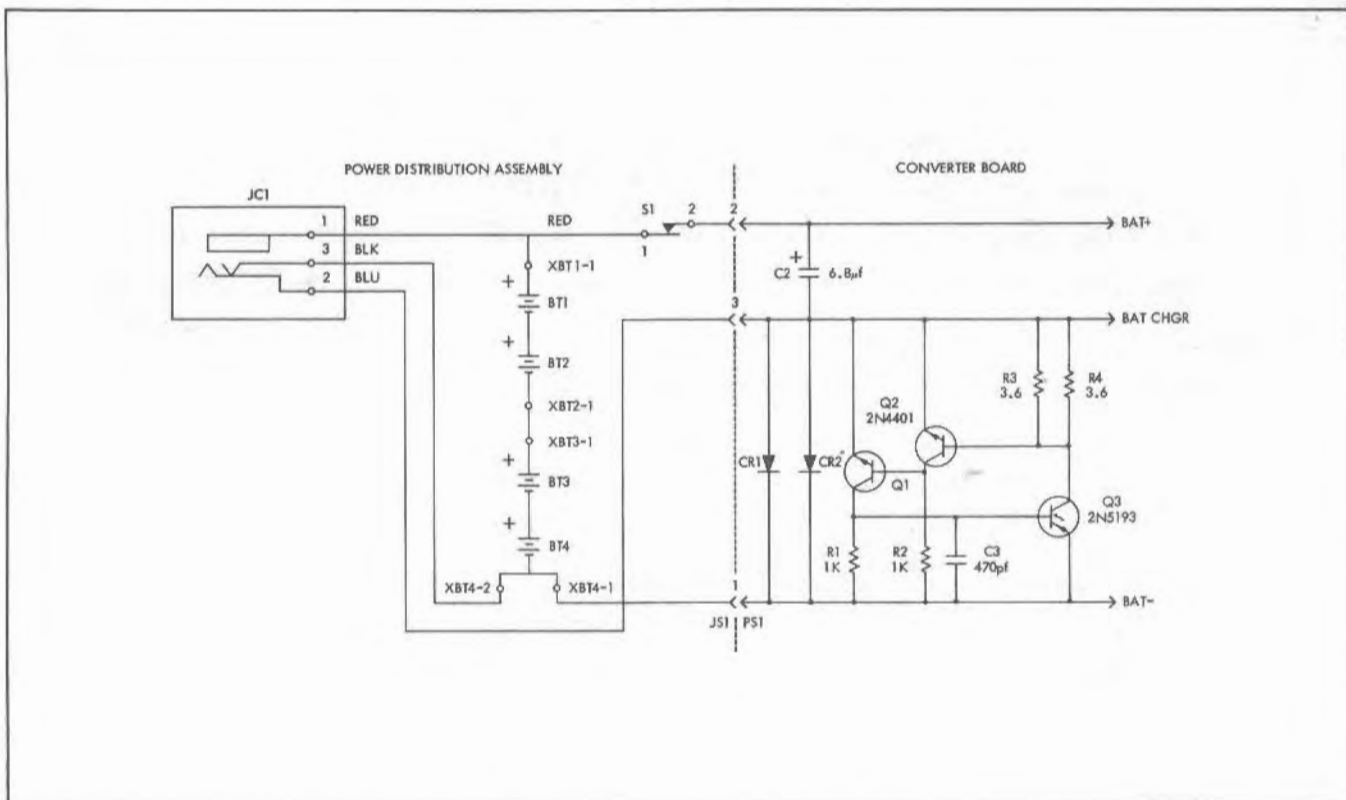


Fig. 2-2 Power Distribution and Battery Charger Schematic

parallel resistors R3 and R4 and through Q3 to the negative battery line, BAT-. The charging rate (300-350 ma) is determined by the voltage drop across R3 and R4.

If the charging current tends to increase, the higher voltage at the base of Q2 causes it to conduct more, which reduces the conduction of Q1. This in turn, lowers the forward bias on Q3, reducing the charging current. The same feedback loop resists any decrease in the charging current. Diodes CR1 and CR2 protect the transistors from reversed voltage and permit uninterrupted operation if the voltage adapter is attached or removed while the computer is busy.

2.2.3 CONVERTER

The Converter board contains the charging current regulator described in Par. 2.2.2 as well as the clock generator, power supply and low battery detector.

2.2.3.1 Clock Generator

Operation of the Converter requires proper operation of the clock circuits; therefore the clock generator is the first part of the Converter discussed. Figure 2-3 is the logic diagram of the clock circuits. The clock circuits generate three clock signals. Clock $\Phi 1$ is used to time certain operations during a portion of the computer bit time. It is also used by Control to generate additional clocks used in selecting bit times within a 20-bit machine cycle. Clock $\Phi 2$ establishes the bit period. Clock ΦR is a reset clock used by the Data File.

A Colpitts oscillator formed by NAND gate Z3C, inductor L1 and capacitors C15 and C16 generates a 1.6 MHz sinusoidal wave. Line CKEN (Clock Enable) is used by factory test equipment to disable the clock for testing and by the 395 Teleprinter Interface to compensate for tolerances in the clock generator. With the assembly installed in the computer CKEN is held at logical 1 by V_{SS} applied through resistor R23, enabling the oscillator. R22 is an isolation resistor to allow injection of an external oscillator signal at CCLK.

Integrated circuit Z1 is a 4-bit shift register, operable as either a serial or parallel register. The logic level at pin 9 determines whether the chip operates as a serial or parallel register. Pin 9 is normally a logical 1, causing Z1 to operate as a serial register. All shifts occur on the positive-going transition of the oscillator signal at pin 10.

Assume that the computer has just been turned on and the register is clear. All flip-flops are in the 0 state and the four true outputs are logical 0. The complemented output $\overline{Q3}$ is connected to the serial inputs of Z1. The Q3 output is logical 0, causing Z3B, pin 6, to be logical 1. The Z3B output is applied to pin 9 of Z1, placing it in serial mode.

On the first positive transition of the oscillator signal, the logical 1 from $\overline{Q3}$ shifts into the Q0 flip-flop. At the second transition, the logical 1 from Q0 shifts into the Q1 flip-flop, while another 1 enters Q0 from $\overline{Q3}$. On the third transition, a 1 enters Q2 from Q1, another 1 enters Q1 from Q0 and a 1 from $\overline{Q3}$ enters Q0. On the fourth transition, 1s shift into all four flip-flops. All four true outputs are now logical 1, while $\overline{Q3}$ is logical 0. On the fifth input transition, the 0 shifts into Q0. The 0 shifts through the register as the 1 did previously. The waveforms at the output pins are square waves which are at the logical 1 level for four oscillator periods, then at logical 0 for four periods. See Fig. 2-4 for waveforms.

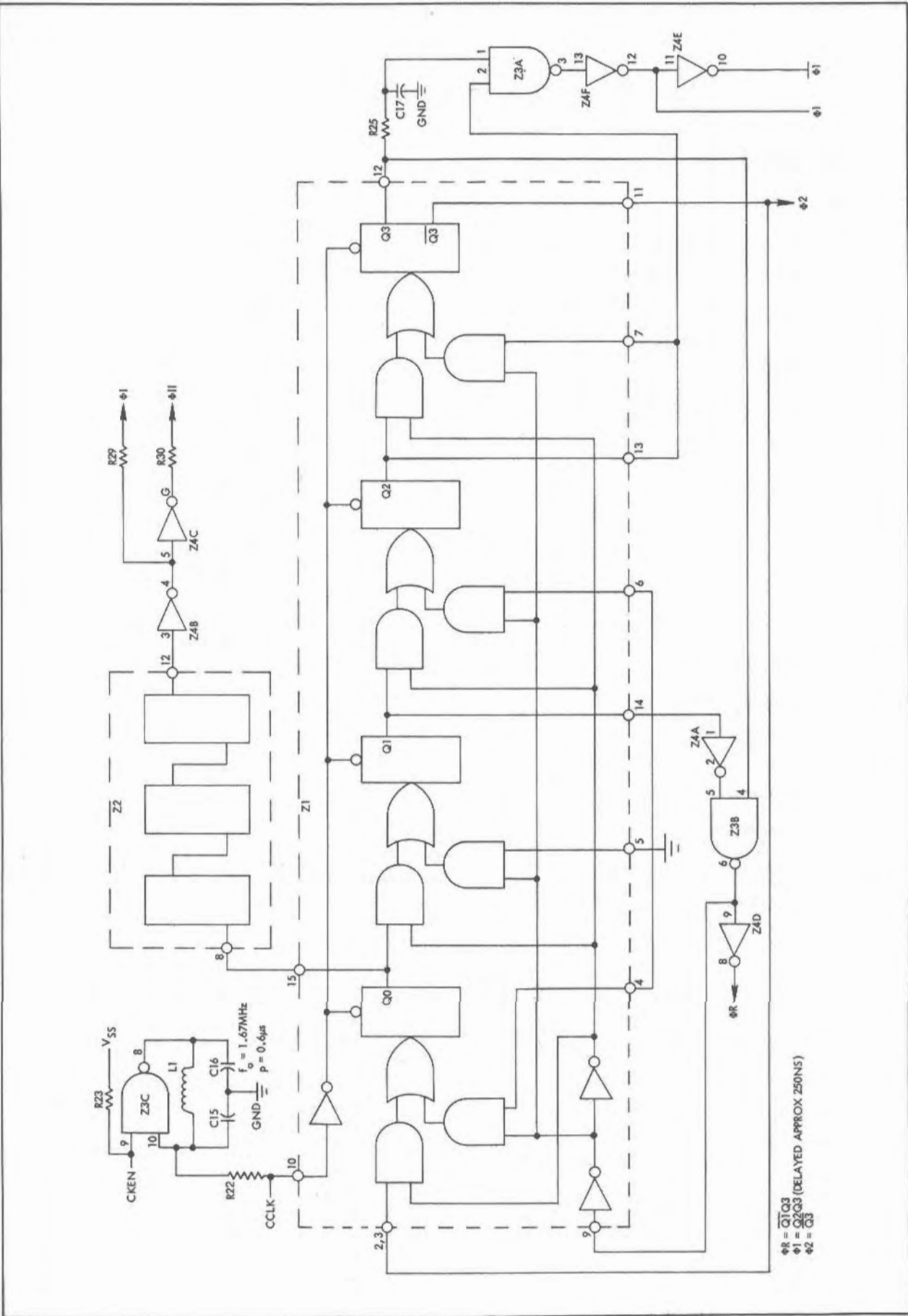
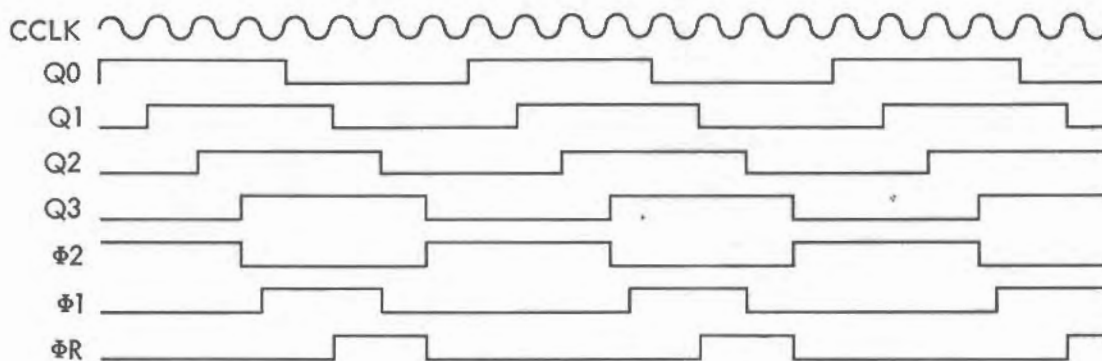


Fig. 2-3 Clock-Generation, Typical Logic Diagram



Notes: 1. Waveforms are idealized. 2. CCLK period is approximately 0.625 microsecond.

Fig. 2-4 Clock Generator Waveforms

The Q1 output is inverted by Z4A and applied to pin 5 of Z3B. The pin 4 input of Z3B is Q3. The output of Z3B goes to pin 9 of Z1. When Q1 is 0 and Q3 is 1, pin 9 of the register is logical 0, changing it from a serial to a parallel register. On the next positive transition at pin 10, the flip-flops load through the parallel inputs instead of making a serial shift. The 0, 1, and 2 inputs are wired to GND, so flip-flops 0, 1, and 2 assume the 0 condition. Input 3 is wired to Q2, so the 1 in flip-flop 2 enters flip-flop 3 just as if the register had shifted serially. As may be seen from the waveform chart, Fig. 2-4, the waveforms are identical to the result of a continuous serial shift; however, if the register should assume an incorrect condition when the computer is turned on or as the result of a voltage transient, the parallel load provision causes a correction within a few microseconds.

The Q3 output is delayed approximately 250 nanoseconds by the RC network comprised of R25 and C17, then applied to the NAND gate Z3A. The other input to Z3A is the Q2 output. Z4E inverts the Z3A output to provide clock $\Phi 1$. $\Phi 1$ is reinverted by Z4E to provide $\overline{\Phi 1}$. The delay of the Q3 output prior to application to Z3A prevents the leading edge of $\Phi 1$ from overlapping the trailing edge of $\Phi 2$.

Clock $\Phi 2$ is the Q3 output of the shift register. Z4D inverts the Z3B output to supply the reset clock ΦR .

Z2, connected as an 8-to-1 counter, counts down the Q0 output to approximately 25 KHz. Z4B is a buffer amplifier which supplies clock ΦI . Z4C inverts ΦI to provide ΦII . Resistors R29 and R30 limit the base current of transistors Q6 and Q7.

2.2.3.2 Multivibrator

The divide-by-8 counter applies ΦI and ΦII to the Converter multivibrator. See Fig. 2-5.

When ΦI is low, Q6 is turned off, V_{SS} , applied through R6 and the transformer winding, turns on Q5. The low level at the collector of Q5 forward-biases Q4, turning it on to allow current to flow through the transformer from terminal 2 to terminal 3.

When ΦI goes to logical 1 and ΦII goes to a logical 0, transistor Q7 turns off and Q8 and Q9 turn on. Current then flows through the transformer from terminal 4 to terminal 3. As the multivibrator switches, the effect is that of a square wave applied across transformer terminals 2 and 4.

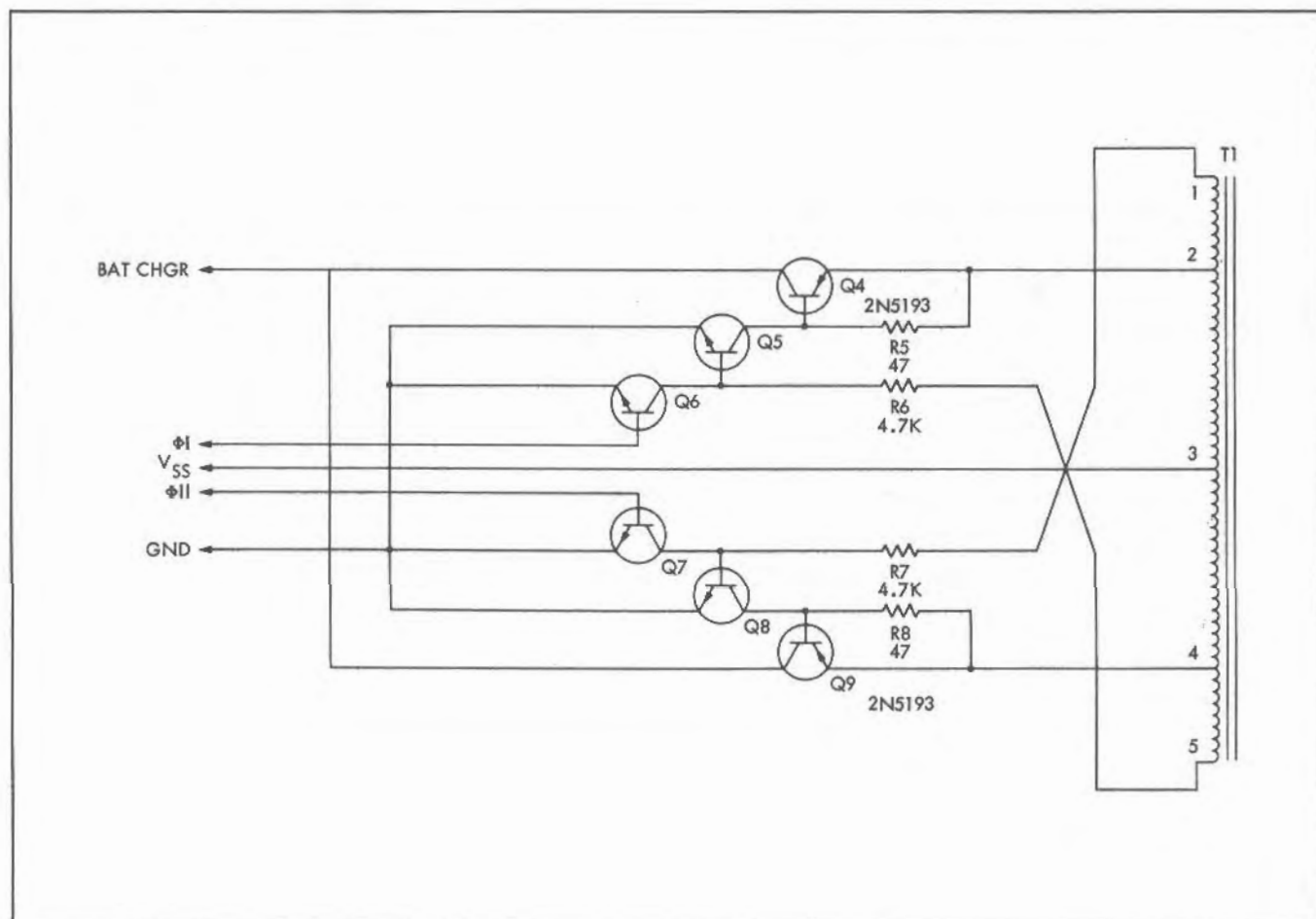


Fig. 2-5 Power Supply Multivibrator Schematic

Resistors R6 and R7 provide a regenerative feedback to speed the switching and ensure that Q4 and Q9 are not both on at the same time. For example, when Q4 turns on, terminal 2 drops to the BAT CHGR potential. Autotransformer action causes terminal 1 to become more negative than BAT CHGR by about 3 volts. This level, applied through R7, results in a strong reverse bias to Q8, holding it completely off. Resistor R8 provides a low-impedance path for any leakage current through Q8 in the off state. The voltage drop caused by any normal value of leakage current through the 47-ohm resistance is insufficient to forward-bias Q9, which turns off.

The feedback from terminal 5 produces the same effect on the other half of the multivibrator when the clock causes it to switch.

2.2.3.3 Low Voltage Supply

The low voltage supply generates the following voltages: V_{BB} , V_{DD} , GND and V_{GG} . See Fig. 2-6 for the schematic of the low voltage circuits. The voltages V_{SS} and BAT CHGR are not generated within the circuit; they come from the batteries or the voltage adapter.

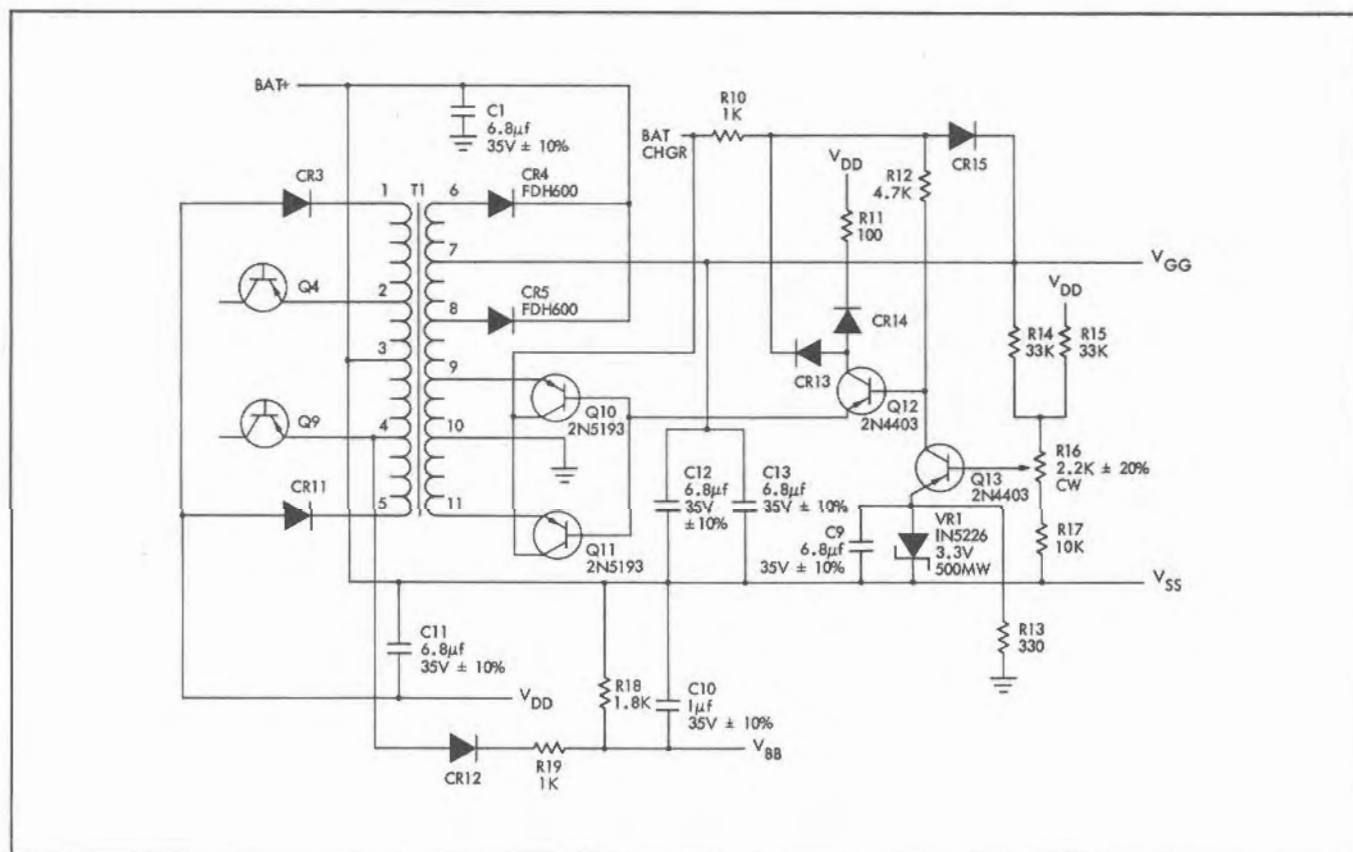


Fig. 2-6 Low Voltage Supply Schematic

2.2.3.3.1 V_{BB} Supply

With the multivibrator operating, the primary of T1 acts as an autotransformer. For example, with Q4 on, terminal 2 is effectively connected to BAT CHGR while terminal 3 is connected to V_{SS} . When a voltage pulse is applied between these terminals, an induced voltage of similar amplitude but opposite polarity is present between terminals 3 and 4. The same action occurs in reverse when Q4 is turned off and Q9 on. Then terminal 2 has a pulse which is 5 volts positive with respect to V_{SS} .

Diode CR12 rectifies the positive peaks at terminal 4. Resistors R18 and R19 limit the potential to which C10 charges by acting as a voltage divider when CR12 is passing a positive pulse. As a result, the DC voltage across C12, which is V_{BB} , is limited to approximately 3 volts. V_{BB} is a bias voltage used by 2K RAM chips.

2.2.3.3.2 V_{DD} Supply

Since the primary of T1 acts as an autotransformer, terminals 1 and 5 produce voltages alternating between approximately 8 volts positive and negative with respect to V_{SS} . Diodes CR3 and CR11 rectify the negative alternations, and C11 filters the output to provide V_{DD} , which is approximately -7.6 volts DC.

2.2.3.3.3 V_{GG} Supply

Transformer secondary terminals 6 and 8 each produce pulses alternating about 16 volts above and below V_{SS} . Diodes CR4 and CR5 rectify the negative alternations, and C12 and C13 filter the rectified voltage to produce V_{GG} , -15 volts with respect to V_{SS} .

2.2.3.3.4 GND Supply

Unlike the other voltage supplies on the Converter board, the GND supply will start without the multivibrator. This is required because the clock generators and the Converter multivibrator require a GND potential to be present before they in turn will operate.

When the power switch is closed, the BAT CHGR line is 5 to 7 volts negative with respect to V_{SS} . The negative voltage, applied through resistors R10 and R12, forward-biases the

base-emitter junction of Q12, which forward-biases Q10 and Q11. (The initial collector drive is established through CR13. Once the multivibrator has started, V_{DD} forward-biases CR14, which provides the collector drive voltage of Q12.)

The collectors of Q10 and Q11 are connected to BAT CHGR, so BAT CHGR is coupled to GND through the transistors and the transformer winding. The voltage applied at BAT CHGR, less the drop across the transistors and the transformer winding, is the GND voltage to enable operation of the clocks and multivibrator.

After the multivibrator has started, a series of negative and positive pulses (with respect to BAT CHGR) are present at terminals 9 and 11. The negative pulses reverse-bias the base-emitter junctions of Q10 and Q11, while the positive pulses forward-bias the junctions. Therefore, Q10 and Q11 now act as diodes to rectify the AC voltages at terminals 9 and 11. Capacitor C1 filters the rectified output from terminal 10.

Winding 9-10-11, Q10 and Q11 are included to produce a 1.2-volt boost to the battery voltage and permit the regulator to generate GND, -5 volts, from a battery voltage which may be as low as 4.4 volts.

NOTE

Unlike most electronic equipment, these machines do not use GND (Ground) as a reference. V_{SS} (BAT+) is the reference voltage in this equipment, and all voltages are with respect to V_{SS} unless specifically stated otherwise. Connecting a load between GND and a negative voltage will result in Q10 and Q11 attempting to pass current in the wrong direction, causing voltage shifts and possible damage.

2.2.3.3.5 Low Voltage Regulator

Transistor Q13, Zener diode VR1, and resistor R13 are the main regulator components. See Fig. 2-6. VR1 holds the emitter of Q13 at a constant level, and R13 maintains a constant current bias. Resistors R17, R14 and R15 establish the initial base potential of Q13. These resistors return to V_{SS} , V_{GG} and V_{DD} , respectively. Any change in the level at the base of Q13 results in a change of collector current, varying the drive to Q12, which in turn controls the bias of Q10 and Q11.

For example, if V_{GG} becomes less negative, either because of a decrease in battery output or change in the components, the forward bias of Q13 decreases, causing the collector to become more negative. The forward bias of Q12, Q10 and Q11 increases, reducing the voltage drop across Q10 and Q11 and causing GND to become more negative. The more negative value of GND causes heavier conduction of the multivibrator transistors in their on condition, increasing the transformer voltages and returning V_{GG} to correct the value.

Potentiometer R16 allows adjustment of the normal operating levels. Changing the setting of R16 varies GND, V_{DD} and V_{GG} simultaneously. R16 is adjusted so V_{GG} is -15.0 to -15.1 volts with respect to V_{SS} .

2.2.3.4 High Voltage Supply

The high voltage supply generates V_{BIAS} and V_{KK} , which are the voltages necessary to operate the display. The circuit consists of two cascaded voltage doublers. Refer to Fig. 2-7 for the following discussion.

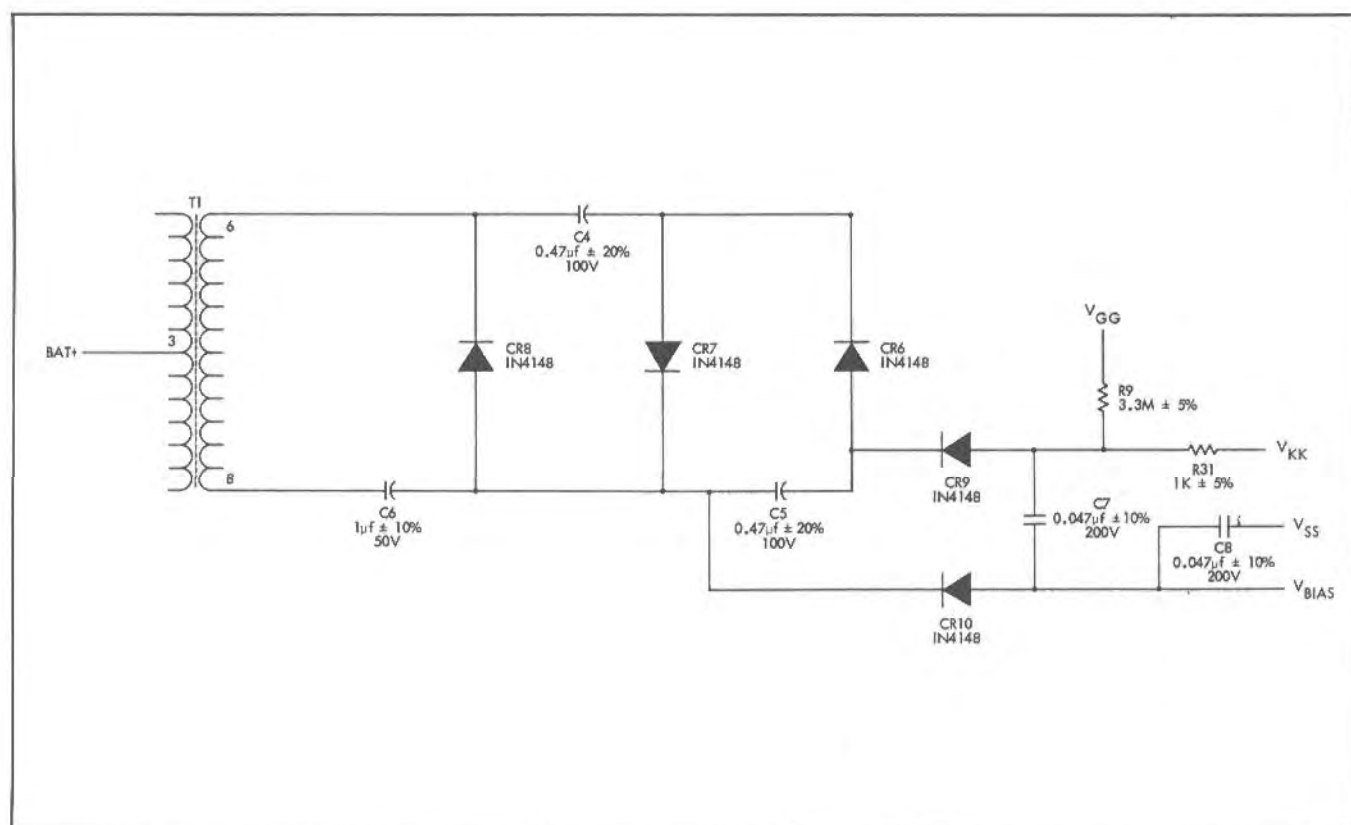


Fig. 2-7 High Voltage Supply Schematic

Transformer T1 produces an output between terminals 6 and 8 which is nominally 32 volts peak-to-peak. Assume the first alternation causes terminal 8 to be 32 volts positive with respect to terminal 6. CR8 is forward-biased, allowing C6 to charge to approximately 30 volts.

On the second alternation, terminal 6 is 32 volts positive with respect to terminal 8. CR7 is forward-biased, which charges C4 to the difference in potential between terminal 6 and the cathode of C6, or 60 volts.

On the third alternation, CR6 and CR8 are forward-biased, which charges C5 to the voltage across C6 and the effective voltage across terminals 6 and 8 of T1, or 60 volts.

The voltage at the anode of CR10 is the sum of the voltage across C6 and peak-to-peak voltage across terminals 6 and 8 of T1, or -60 volts, which is the V_{BIAS} voltage. The voltage at the CR9 anode is the sum of the voltage across C4 through C7, or -120 volts, which is the V_{KK} voltage.

R9 is a discharge resistor which allows C7 and C8 to discharge after power is removed from the computer. R31 prevents damage to the voltage doubler circuit should a short develop between V_{KK} or V_{BIAS} and GND. R31 also prevents damage to the panaplex display from high-voltage spikes on the V_{KK} line.

2.2.3.5 Low Battery Detector

The low battery detector supplies a signal which provides an indication to the operator when the batteries are nearly discharged. The circuit is illustrated by Fig. 2-8.

Resistor R20 biases the base of Q14 to the BAT CHGR level. The emitter of Q14 is supplied by GND, and the collector of Q14 is supplied by V_{SS} through R21. When the computer is operating from fully charged batteries, the emitter-base junction of Q14 is reversed-biased by GND and BAT CHGR being approximately the same level. Q14 is cut off, and $\overline{INL2}$ is held to a logical 1 by V_{SS} across R21.

As the batteries discharge, the bias on the base of Q14 goes more positive, and Q14 begins to conduct. When BAT CHGR level goes to approximately -4.4 volts, Q14 conducts shorting $\overline{INL2}$ to GND, indicating the batteries need charging.

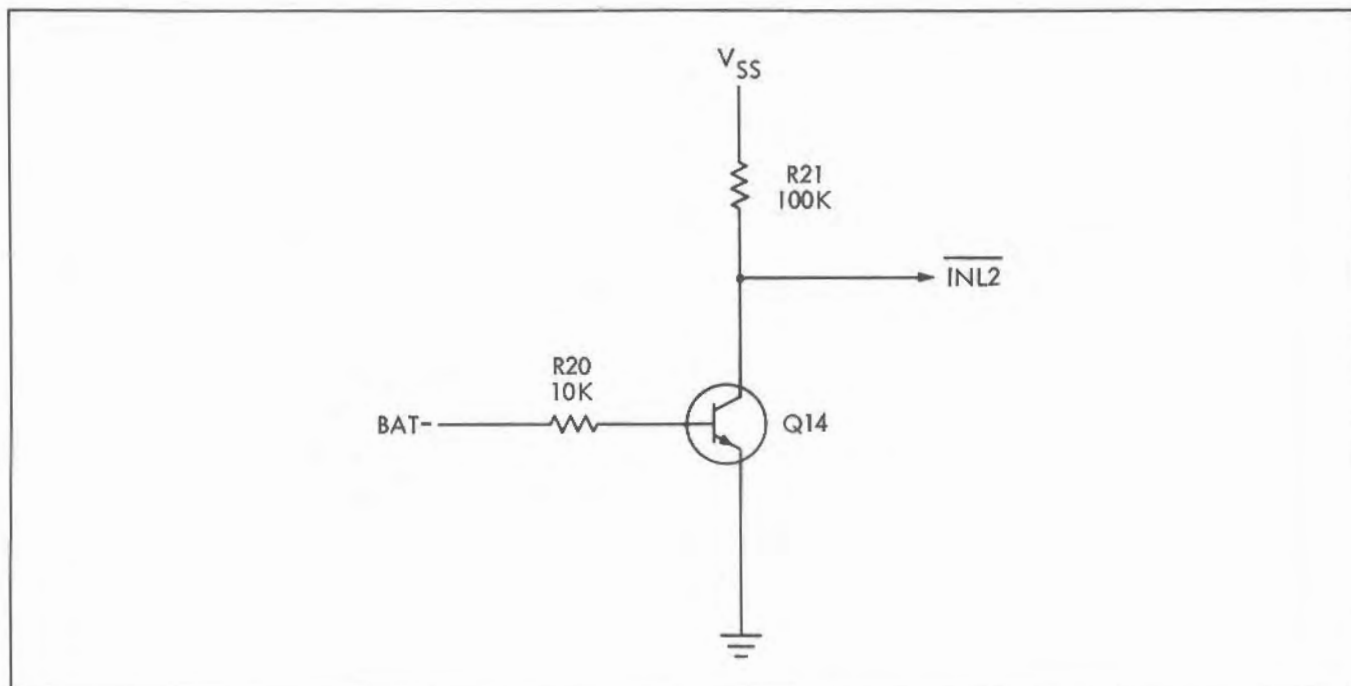


Fig. 2-8 Low Battery Detector Schematic

$\overline{\text{INL2}}$ goes to the Keyscanner chip on the Display Drive board. The Keyscanner chip converts $\overline{\text{INL2}}$ to a machine code which is then sent to the Control board. When $\overline{\text{INL2}}$ goes low, the idle program flashes the display indicating the batteries have only enough power for a few minutes of operation.

2.3 KEYBOARD AND KEYSKANER PRINCIPLES OF OPERATION

The computer contains a highly sophisticated means of detecting and encoding switch closures. Since all circuitry performing this operation is contained on the Display Drive board, with the exception of the switches themselves, most of the following discussion treats the keyboard and keyscanner portion of the Display Drive board as a single unit.

2.3.1 KEYBOARD

All models use electrically identical keyboards, which contain 43 momentary action pushbutton switches and five slide switches. With the 392 Cassette Drive connected to the computer, the READ FROM TAPE and WRITE ON TAPE switches on the Cassette Drive keyboard are also part of the Keyscanning circuit. The keyboard insert covers switches not used by the computer. Figure 2-9 is the schematic diagram of the keyboard.

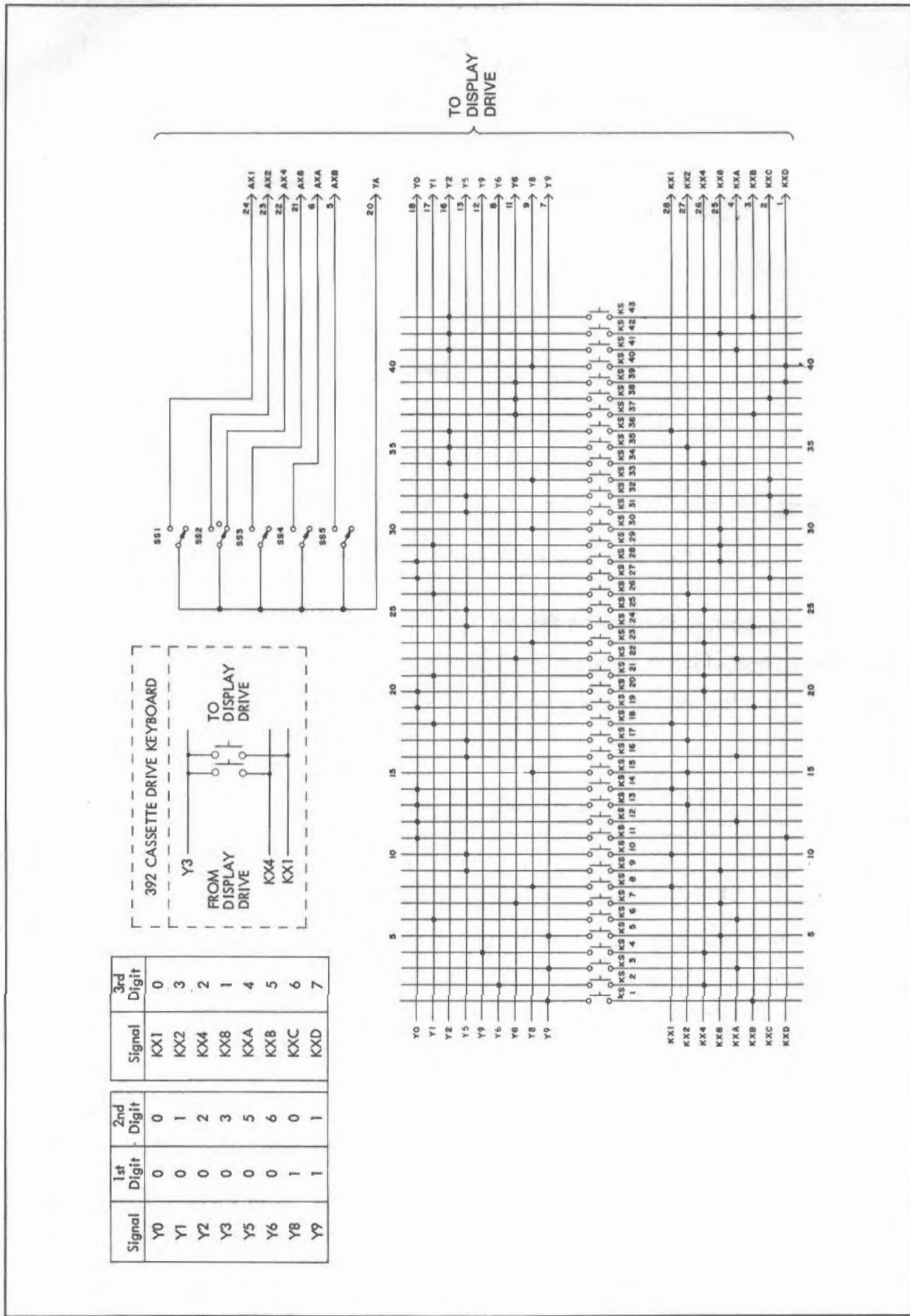


Fig. 2-9 Schematic Diagram, Keyboard

The keyscanner circuitry transmits eight sampling pulses on the input lines labelled with the decimal designators Y0, Y1, Y2, Y3, Y5, Y6, Y8, and Y9. A ninth pulse enters on line YA. A closed switch allows a sampling pulse to return to the keyscanner on one of the output lines. YA pulses passing through a closed slide switch return to the keyscanner via the lines marked AX1 through AXB. A closed key switch allows a pulse to return to the keyscanner on one of the lines labelled KX1 through KXD.

The keyswitches operate by distorting the shape of a metal dome so it closes a circuit between an input and an output line. See Fig. 2-10. The dome is installed concave side down on a pair of concentric printed circuit lands. When the operator presses the key, the actuator presses downward against the dome, causing the center to bend toward the printed circuit board. When the key is fully depressed, the center of the dome contacts the inner printed circuit land, completing the connection between the input and output lines.

The slide switches are comprised partly of contacts on the keyboard printed circuit board and partly of contacts on a movable assembly held captive by the actuator holder.

Table 2-1 tabulates the keyswitch functions of the computer. Table 2-2 does the same for the slide switches, and Table 2-3 tabulates the keyswitch functions of the 392 Cassette Drive.

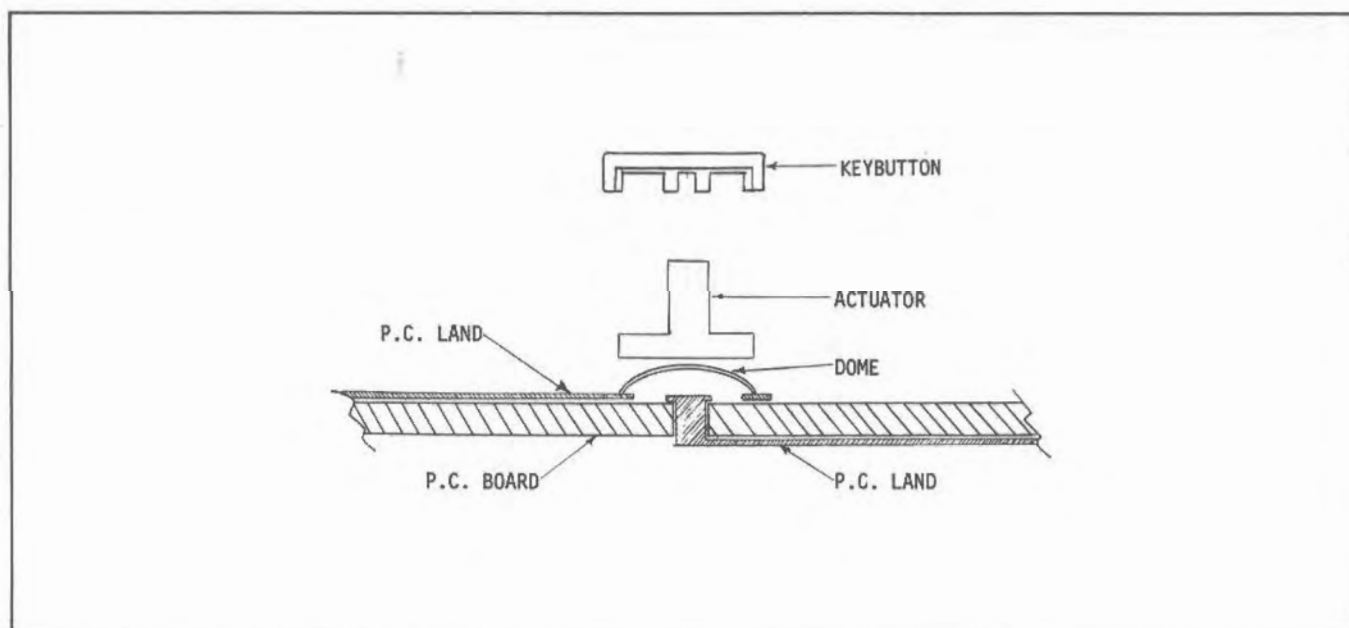


Fig. 2-10 Key Switch Construction

Table 2-1
KEY SWITCH FUNCTIONS












































Switch	Code	Legend	Switch	Code	Legend	Switch	Code	Legend
		Scientist			Scientist			Scientist
KS1	115		KS16	054		KS30	101	
KS2	062		KS17	051		KS31	057	
KS3	114		KS18	010		KS32	056	
KS4	112		KS19	005		KS33	106	
KS5	111		KS20	002		KS34	022	
KS6	014		KS21	012		KS35	023	
KS7	061		KS22	064		KS36	020	
KS8	100		KS23	102		KS37	065	
KS9	053		KS24	055		KS38	066	
KS10	050		KS25	052		KS39	067	
KS11	007		KS26	013		KS40	107	
KS12	004		KS27	006		KS41	024	
KS13	003		KS28	001		KS42	021	
KS14	000		KS29	011		KS43	025	
KS15	103							

Table 2-2
SLIDE SWITCH FUNCTIONS

Switch	Legend Scientist
SS1	GRAD/DEG
SS2	RUN/STEP/LOAD
SS3	NOT USED
SS4	NOT USED
SS5	PROGRAM/REGISTERS

Table 2-3
CASSETTE DRIVE SWITCH FUNCTIONS

Switch	Code	Legend
K1	032	WRITE ON TAPE
K2	030	READ FROM TAPE

2.3.2 KEYSKANER CHIP ACL-02/TCL-02

Keyscanner chips come in two versions: on ACL-02 manufactured by American Microsystems, Inc., and a TCL-02 manufactured by Texas Instruments, Inc. The two chips operate identically, but are not interchangeable because of different pin connections. However, a Display Drive board using the ACL-02 may replace a Display Drive board using the TCL-02 and vice versa.

The Keyscanner schematic, Fig. 2-11, contains a functional block diagram of the chip. Pin numbers for both versions are shown; for example, the T4, A16 marking for the IXDI output means that this signal is at pin 4 of the TCL-02 and at pin 16 of the ACL-02.

Control transmits instructions serially to the Next Instruction Register in the Keyscanner chip via the CTRL line. When the chip finishes executing the previous instruction, the new instruction transfers in parallel to the Execution Register. The Instruction Decode Logic decodes the contents of the Execution Register and uses the results as control signals for the chip logic. As the chip

decodes and executes the instruction, Control transmits a new instruction in serial form to the Next Instruction Register. Thus, the chip has a look-ahead capability in that it may accept a new instruction while in the process of executing an earlier one.

The CTRL0 logic generates control instructions for other chips and transmits them to the common control buss, CTRL. The PWON logic accepts the PWON signal generated when the computer is first turned on and sets the chip logic to the required initial conditions as the computer executes the Power-On routine.

The DIS0 input is normally disconnected, but may be jumpered to V_{SS} when it is desirable to disable the chip outputs for test purposes. When DIS0 is at logic 1 (V_{SS}), the DIS0 logic disables all output gates in the chip. The special clip-on adapter used for troubleshooting applies the output disabling signal to the original chip when placing a substitute chip in parallel with the original.

2.3.3 KEY SWITCH SCANNING

The Y-Scanner in the ACL-02/TCL-02 continually transmits sampling pulses to the keyboard via lines Y0 through Y9. Each of the Y lines connects to several key switches. Each of the KX lines connects to the opposite side of several key switches so that each switch represents a unique intersection of a Y line and a KX line.

The Y-Scanner contains a counter and decoder to generate the sampling pulses. The first pulse from the scanner is the Y0 pulse, followed by the Y1 through Y9 pulses in sequence. When the operator presses a key, one of the Y pulses re-enters the Display Drive board via a KX line, passes through the isolation diode in that line, enters the Input Register on one of the X lines, and sets an input status bit, INL1.

During the Idle routine, the computer periodically executes the Read Input Status (RINSO operation which causes the input status bits to be read into the Input Register, shifted through the Output Selector to IXD1 and into the Index Register on the Control board. The computer uses seven status lines. $\overline{INL2}$ is discussed in Par. 2.3.3.5 $\overline{INL8}$, $\overline{INH1}$, $\overline{INH2}$, $\overline{INH4}$, and $\overline{INH8}$ are discussed in Par. 2.6. When Control senses that the INL1 bit is set, the computer branches to the Read Key microprogram.

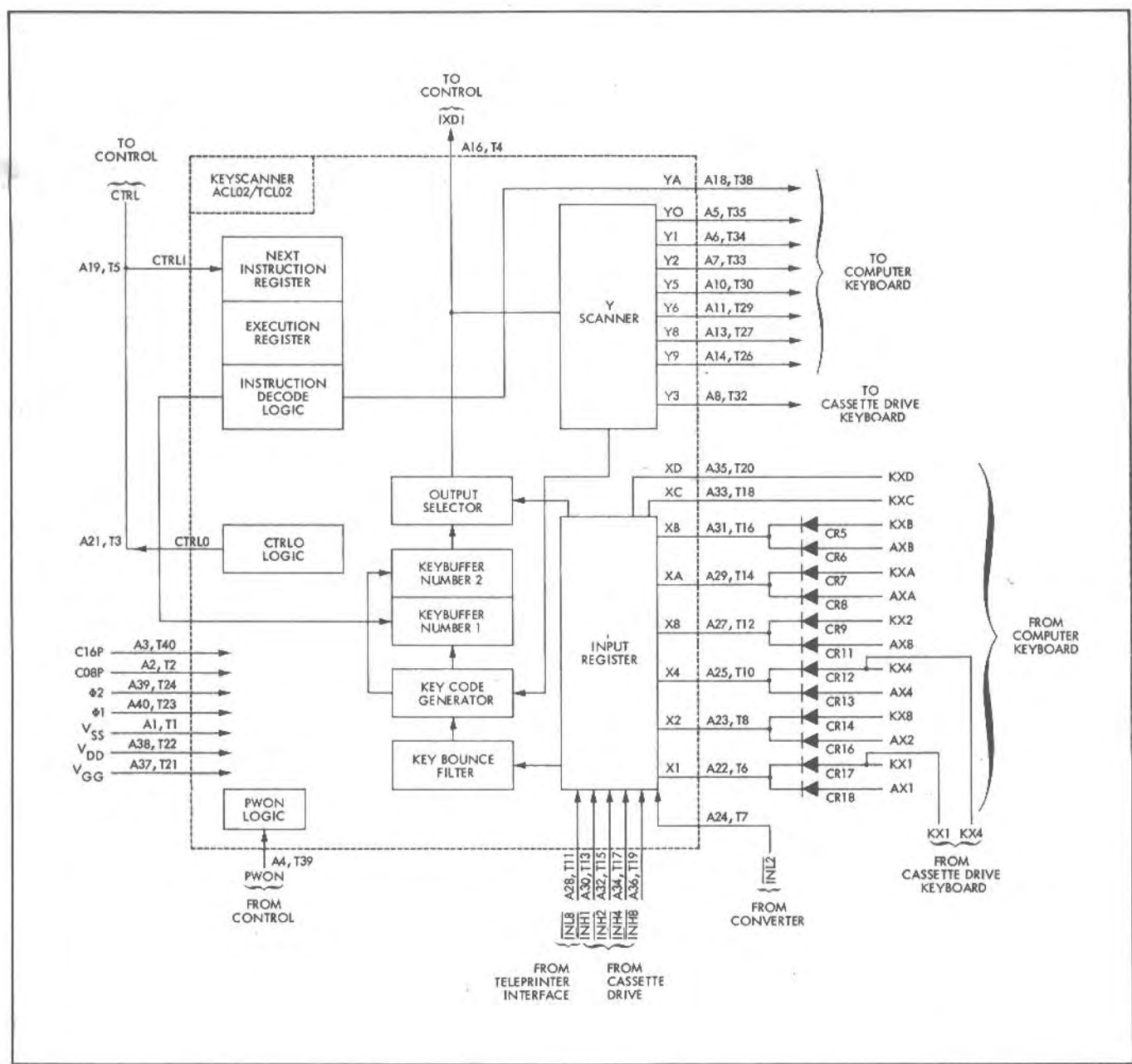


Fig. 2-11 Keyscanner Schematic

The Input Register is an 8-bit parallel-to-serial converter with each bit corresponding to a particular input line. When a key switch closure is detected, the internal logic of the chip stops the counter in the Y-Scanner and initiates a parallel transfer from the input register to the Key Code Generator.

The Key Bounce Filter, between the Input Register and the Key Code Generator, is a digital register which introduces a predetermined delay in the transfer. The Power-On routine programs

the filter for a specified delay when the computer is first turned on. Without the filter, key bounce could cause multiple entries or result in error.

The Key Code Generator combines the contents of the counter in the Y-Scanner with the contents of the Input Register to produce an 8-bit binary code, which is the instruction code for the operation represented by the key pressed. The count of the Y-Scanner and the position of the bit from the Input Register determine the code generated. The Y count determines the first two digits of the octal code while the third digit is established by the specific KX line by which the pulse returned to the Keyscanner. Instruction codes are normally expressed octally while the computer uses their binary equivalents. The insert to the Keyboard schematic diagram, Fig. 2-9, shows how the key codes are constructed by the combination of the Y and KX lines.

The Key Code Generator output transfers parallelly to Key Buffer Number 1, then makes a second transfer to Key Buffer Number 2. The computer then executes a Read Key instruction, which shifts the contents of Key Buffer Number 2, via IXDI, to the Index Register on the Control board. While the contents of Key Buffer Number 2 are shifting out, a new key code may transfer into Key Buffer Number 1, permitting faster keyboard operation.

Exceptions to this buffering are the codes for Reset and Clear. When the Key Code Generator assembles the code for either of these operations, the code transfers directly to Key Buffer Number 2 by a separate path. The reason for this is explained in the following paragraphs in conjunction with the Error routine.

When the operator performs an illegal operation by calculating an answer exceeding the limits of the memory, the computer jumps to the Error routine. Instructions from Control cause the input to Key Buffer Number 1 to lock up and prevent the normal transfer of key codes from the Key Code Generator. The Control does not transmit the RINS instruction, so key codes are ignored.

Depressing the RESET or CLEAR key places the code for Reset or Clear in Key Buffer Number 2, bypassing Key Buffer Number 1. The CTRL0 Logic generates and transmits a pulse to Control. This pulse occupies a unique time slot in the cycle period and appears in that slot only when RESET or CLEAR has been depressed. When Control detects the pulse, it interrupts the Error routine, reads the key code, and executes the Reset or Clear microprogram.

2.3.4 SWITCH GROUP A-SCANNING

During part of the routine, the computer executes the Read Switch Group A (RSWA) instruction. Switch Group A consists of the five slide switches on the keyboard. When the RSWA command is executed, the YA pulse passes to the AX lines through the closed slide switches and into the Input Register, where it sets bits corresponding to the switches which are closed. The Input Register contents then shift serially through the Output Control, to IXDI, and are read into the Index Register on the Control board.

As a result of the Switch Group A settings, the computer modifies its operation according to microinstructions written into the ROM memory. For example, closing SS1 on a Scientist model affects only the trigonometric functions, causing the computer to interpret angle units as gradients rather than degrees. On the other hand, closing SS5 causes the content of program memory rather than data memory to be written on a peripheral device. See Table 2-2 for Switch Group A functions.

2.4 DISPLAY AND DISPLAY CONTROL PRINCIPLES OF OPERATION

Three assemblies have a major role in displaying the results of numeral entries or calculations. They are the display assembly, the display interconnect and the display control portion of the Display Drive board. The display interconnect simply provides the connections between the display control circuits and the display assembly.

2.4.1 DISPLAY ASSEMBLY

The display assembly operates in a multiplexed mode wherein the cathode drive and decode logic are time-shared among all the digit positions. The display has ten cathode connections: seven segment connections, a decimal point connection and two comma connections. Each digit has a separate anode connection. The characters are displayed by successively applying positive potentials to the anodes corresponding to digit positions while applying negative potentials to the appropriate cathode busses. See Fig. 2-12 for the display connections and segment configuration.

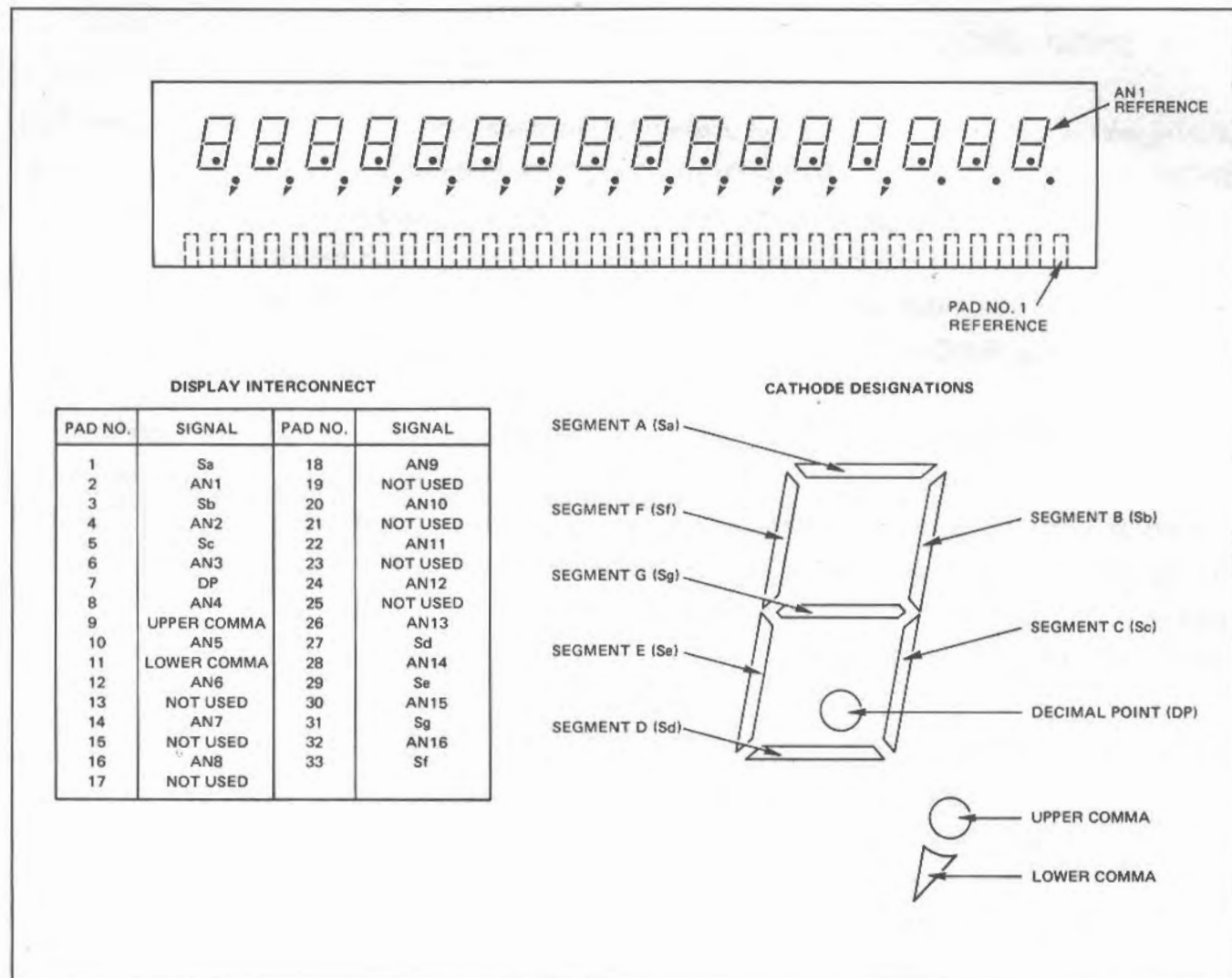


Fig. 2-12 Panaplex II Display Assembly

2.4.2 DISPLAY ENCODER CHIP ACL-08/TCL-08

Display Encoder chips come in two versions: an ACL-08 manufactured by American Microcircuits, Inc., and a TCL-08 manufactured by Texas Instruments, Inc. The chips operate identically, but are not interchangeable because the pin connections differ. However, a Display Drive board using the ACL-08 may replace a Display Drive board using the TCL-08 and vice versa. Refer to the display control schematic, Fig 2-13, for the following discussion.

Control transmits control instructions via CTRL to the Next Instruction Register in the Display Encoder chip. After an instruction has entered the register, it transfers in parallel to the Execution Register, where the Instruction Decode Logic converts the instruction to control signals for

the other logic circuits within the chip. The Instruction Decode Logic also receives inputs from the sixteen-bit control word store and an external timing signal, C16P. While the instruction in the Execution Register is being decoded and executed, a new instruction is being shifted into the Next Instruction Register, eliminating the need for the logic to wait while a new instruction shifts into the chip.

The sixteen-digit Display Register stores the number to be displayed and provides an input to the Anode Time, Comma Comparator. The Anode Time, Comma Comparator controls the timing of Anode Select Register and determines the placement of commas and the decimal point in the display. The Display Register transfers the number, one digit at a time, to the Segment Encoder.

2.4.3 DISPLAY CONTROL OPERATIONAL DESCRIPTION

When the Display Encoder chip receives an output instruction from Control, it enables cathode and anode select lines. The following example is for a Scientist model displaying the number 67 with the decimal point set at 0.

The Anode Select Register enables the anode select lines in the following sequence: $\overline{DA4}$, $\overline{DA7}$, $\overline{DA10}$, $\overline{DA13}$, $\overline{DA0}$, $\overline{DA3}$, $\overline{DA6}$, $\overline{DA9}$, $\overline{DA12}$, $\overline{DA15}$, $\overline{DA2}$, $\overline{DA5}$, $\overline{DA8}$, $\overline{DA11}$, $\overline{DA14}$, and $\overline{DA1}$. The Anode Select Register first enables DA3 to display the 6. The enable signal, approximately -8 volts, turns on transistor Q16. With Q16 on, V_{SS} is applied through Q16 to AN4. At the same time the Segment Encoder selects the segments to display the 6.

When a specific segment is unselected, the select line from the Display Encoder chip remains at -8 volts. The -8 volts forward-biases the cathode drive transistor for that segment, placing the collector at nearly V_{SS} . An isolation diode applies -120V to the cathode buss of the display assembly. The -120V is less than the ionization potential of the glow tube, so the segment remains off.

When the segment is selected, that line from the Display Encoder chip rises to V_{SS} , turning off the drive transistor. A coupling capacitor couples this transition to the display cathode connection, superimposing the -60V on the -120V already present. At the same time, the anode in the selected digit position rises from -38V to V_{SS} as a result of the anode drive transistor turning on. The potential across the anode and the selected cathode segment becomes approximately 180V, sufficient to ionize the glow tube.

The coupling capacitor discharges almost immediately after the glow tube ionizes; however, the -120V applied through the diode is sufficient to maintain the glow as long as the anode remains at V_{SS} .

The first digit position enabled being $\overline{DA3}$, anode transistor Q16 turns on as the Segment Encoder selects the appropriate cathodes to display the numeric 6: S_a , S_c , S_d , S_e , S_f , and S_g . These segments turn on at display position AN4, and remain on while this position is enabled.

At the end of the digit time, $\overline{DA3}$ returns to V_{SS} , blanking the digit. The Anode Select Register advances through the sequence listed above until it comes to the next digit to be displayed, DA2.

Since the character for $\overline{DA2}$ is a numeric 7, the Segment Encoder selects cathodes S_a , S_b , and S_c as Q3 applies V_{SS} to anode AN3.

The last position enabled is $\overline{DA1}$. Q2 applies V_{SS} to AN2 as the Segment Encoder selects the DP cathode.

Each character remains lighted only a small fraction of the time; however, the cycle repeats frequently enough that the display appears to glow continuously.

2.5 CONTROL PRINCIPLES OF OPERATION

Control is the heart of the computer. It executes the ROM micro-instructions and contains the adder circuits and the input/output control logic. The Control Assembly also contains the I/O connector, which allows communication with peripheral devices.

Control is comprised of four MOS/LSI chips, with few discrete components. Because of the complexity of these chips (more than 1000 logic gates per chip), the description is restricted to the block diagram level. For the following discussion, use the Control block diagram, Fig. 2-14.

The Control board may use either of two chip sets: an ACL series manufactured by American Microcircuits, Inc., or a TCL series manufactured by Texas Instruments, Inc. The two types operate identically (e.g., the ACL-07 and the TCL-07 are functionally equivalent), but have

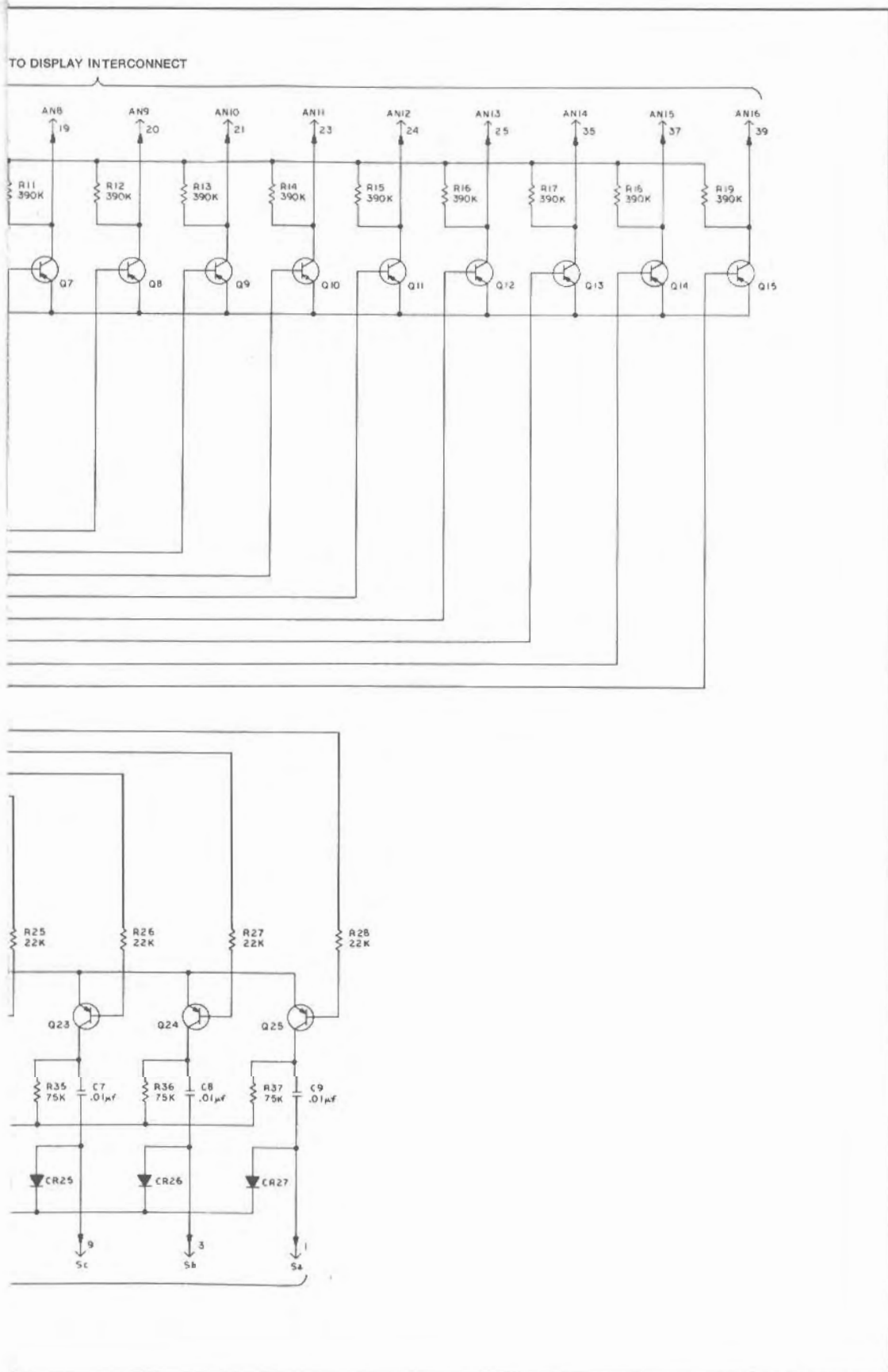
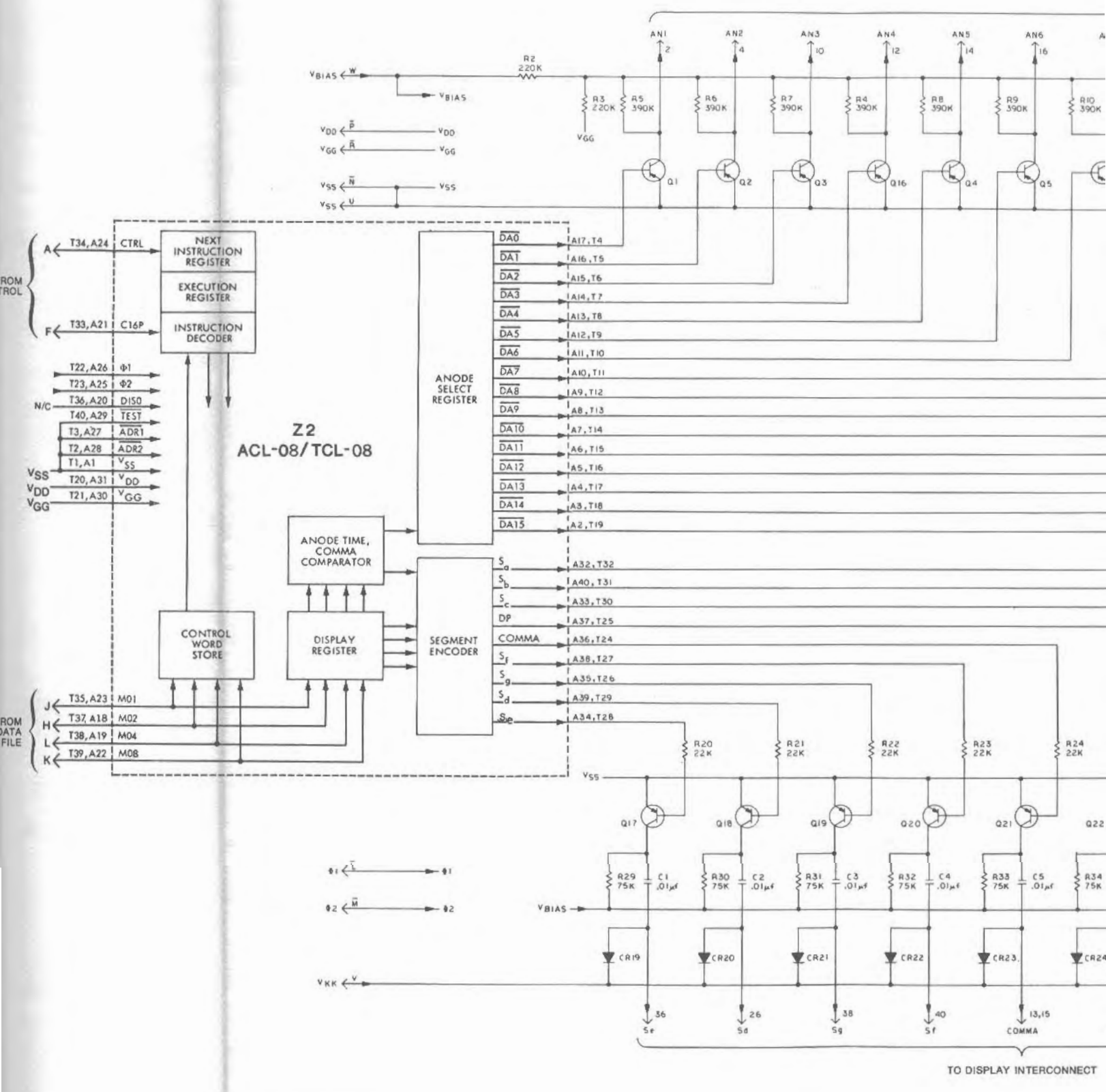


Fig. 2-13 Display Control Schematic Diagram



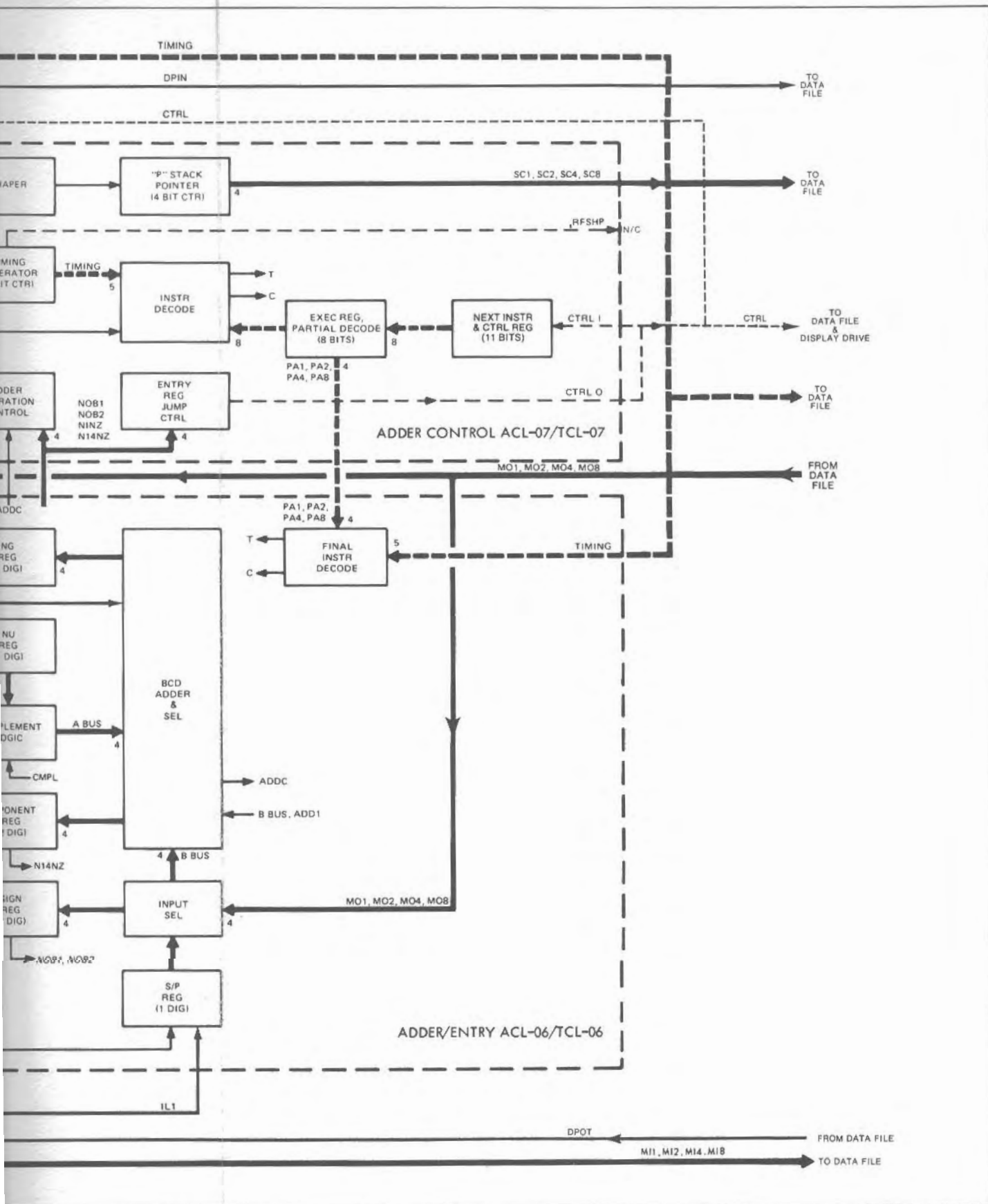
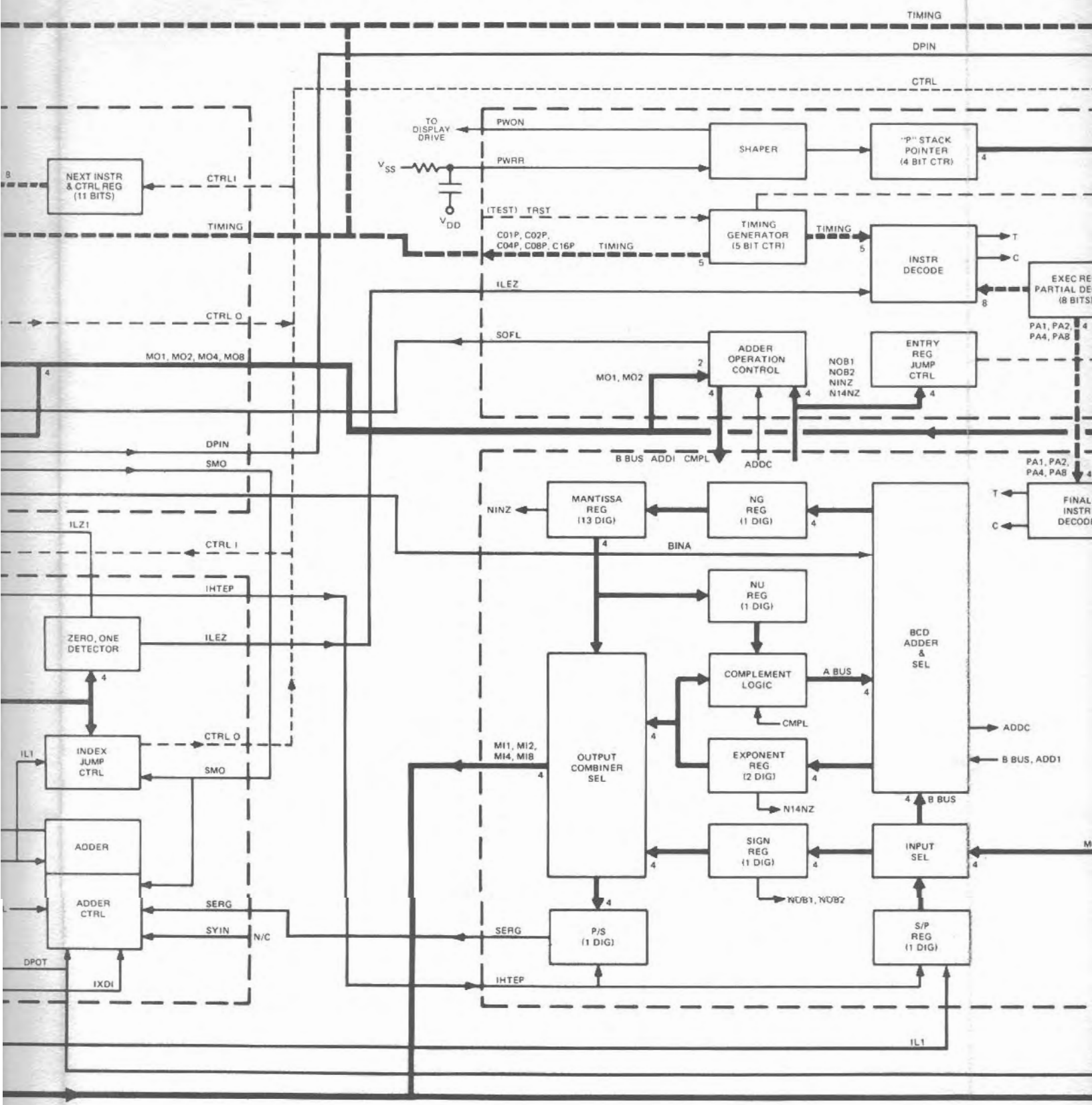
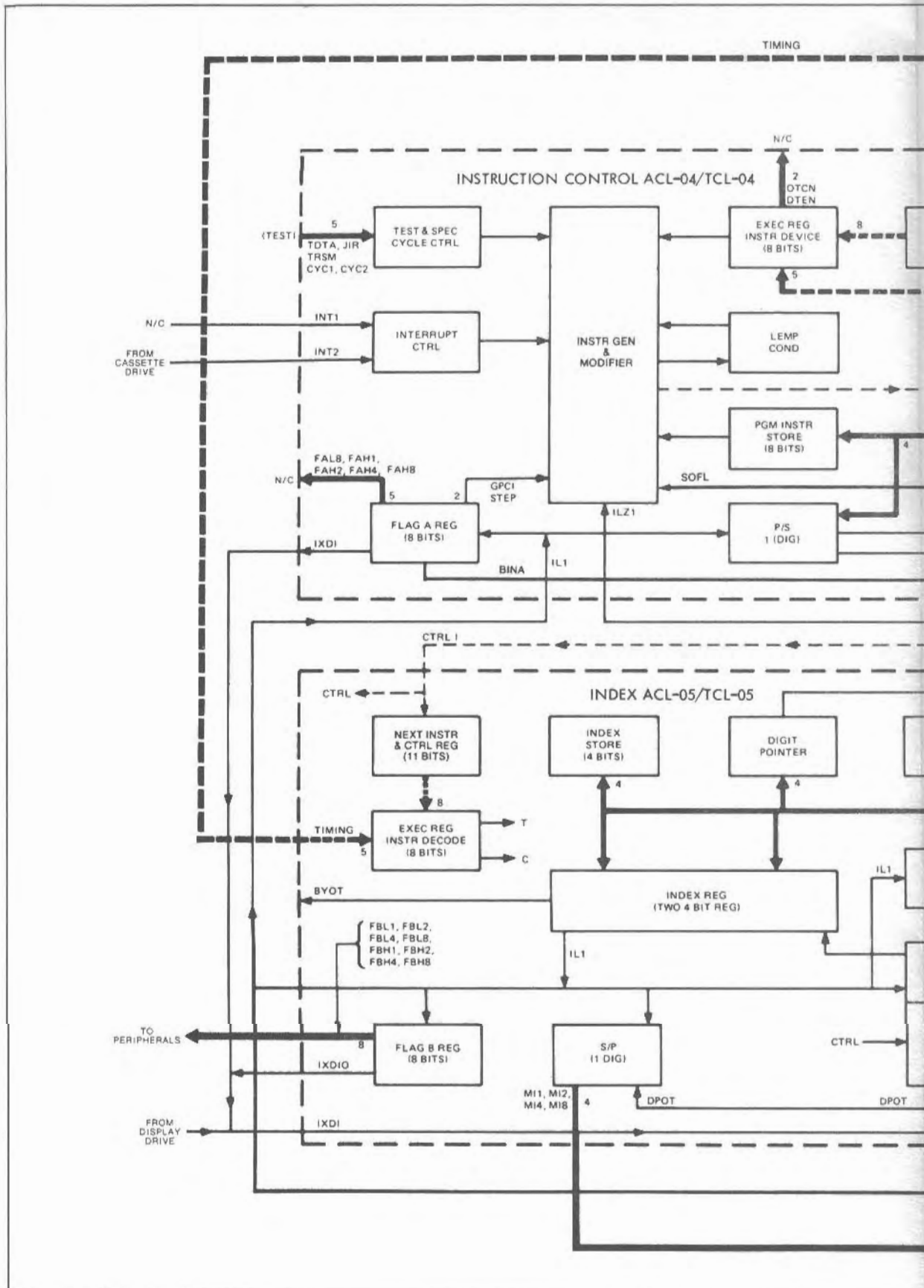


Fig. 2-14 Control Block Diagram





different pin connections. An ACL series chip cannot replace a TCL series chip, but a Control Board using ACL chips may be exchanged for one using TCL chips and vice versa.

2.5.1 INSTRUCTION CONTROL CHIP ACL-04/TCL-04

The primary function of the ACL-04/TCL-04 is conversion of machine instruction codes into control instructions for the other combinational logic chips.

Control instructions from other chips enter the Next Instruction Register in serial mode and then shift in parallel to the Execution Register, where the Instruction Decoder converts them into control signals for the chip logic. While one instruction is being decoded and executed, the next instruction is shifting into the Next Instruction Register.

The Program Instruction Store provides temporary storage for micro-instructions received from the ROMs via the memory output lines, M01, M02, M04 and M08. The Instruction Generator and Modifier converts these codes into control signals for the other chips.

The Parallel-to-Serial Converter also receives inputs from the memory output lines, as well as a serial input from IL1. It converts these inputs to the serial outputs DPIN (Data Pointer In) and SMO (Serial Memory Out).

The Flag A Register is an 8-bit register for storage of status bits used to modify computer routines. The Flag A Register receives its input from the Index Register via IL1. Two bits are used internally in the ACL-04/TCL-04. GPCI changes the response of the Instruction Generator and Modifier from keyboard codes to micro-instruction codes. STEP causes the machine to halt after execution of each key micro-instruction; it is used in factory testing only. The computer uses only one Flag A bit external to the Instruction Control chip. BINA (Binary Add) changes the adder logic of the ACL-06/TCL-06 from a BCD (Binary-Coded-Decimal) adder to a straight binary adder.

The remaining Flag A Register output, IXDI, is used in executing the Read Flag Group A (RFGA) instruction. RFGA shifts the contents of the Flag A Register to the Index Register via IXDI.

The Test and Special Cycle Control circuits are used only in factory testing. The Interrupt Control is used by the computer to communicate with peripheral devices. When the interrupt is generated by a peripheral device, the computer branches to the interrupt microprogram.

2.5.2 INDEX CHIP ACL-05/TCL-05

The Index chip contains registers, decoders, an Adder Control and an Adder circuit for operations on the Index Register.

The Index Register is an 8-bit register divided into two sections, called Index High (IH) and Index Low (IL). The sections may be used independently or as a single 8-bit register. IH may be exchanged with IL. The Index Register may operate as either a serial or parallel register.

Index Store (IS) is a separate 4-bit register which provides temporary storage of the contents of IH or IL.

The Flag B Register is used for peripheral control. By software manipulation of Flag Group B, the computer controls the operating status of the peripheral devices. Par. 2.6 describes peripheral system controls.

The Digit Pointer is basically a time comparator which generates IHTEP. This signal determines the digit position from IH and signals the correct time to transfer the contents of IL to the Entry Register or the selected digit from the Entry Register to IL.

The Zero, One Detector decodes the contents of IL and provides two outputs for use during the Add and Repeat (ADRP) instruction. ILEZ (Index Low Equals Zero) goes to the Adder Control chip and is used in repeated operations in which IL is decremented to tell the Adder Control when to stop. ILZ1 (Index Low Equals 1) goes to the Instruction Control Chip to terminate the ADRP instruction.

The Adder Control and Adder circuits perform various logic operations on the Index Register.

The Serial-to-Parallel Converter changes the serial signals IL1 and DPOT to parallel memory inputs.

The Execution Register stores an instruction while the Instruction Decoder generates the internal control signals from the instruction. The Next Instruction Register provides a look-ahead capability, allowing the next instruction to shift in while the current instruction is executing.

2.5.3 ADDER CONTROL CHIP ACL-07/TCL-07

The Adder Control chip shares the function of controlling the BCD Adder circuitry with the Adder/Entry chip (ACL-06/TCL-06). It also generates the PWON signal and several timing signals.

As in the other chips, the control instructions shift serially into the Next Instruction Register, then transfer to the Execution Register, where the Partial Decode circuitry begins the decoding process. The partially decoded outputs go to both the Instruction Decoder within the Adder Control chip and to the Final Instruction Decoder in the Adder/Entry chip.

When the computer is first turned on, an RC network generates a ramp signal, PWRR. The Shaper converts PWRR into a sharply-defined digital pulse, PWON, which resets the logic in the Keyscanner chip, ACL-02/TCL-02. The Shaper also generates a signal to reset the P-Stack pointer. As a result of the PWON signal, the computer branches to the Power-On routine.

The P-Stack Pointer is an up-down counter which keeps track of the P-stores used when a branch instruction is executed. The actual P-store is in the RAM memory. The output signals (SC1, SC2, SC4 and SC8) go to the Memory Address chip for conversion into addresses.

The Timing Generator uses the basic timing signal $\Phi 1$ to generate five additional timing signals, C01P, C02P, C04P, C08P and C16P. Paragraph 2.8 contains additional information about these clocks.

The Adder Operation Control tests a number of signals and transmits commands to the Adder/Entry chip as a result of the inputs. Data File output signals M01 and M02 are used by the Adder Operation Control to determine whether it is necessary to perform a complement operation. M01 carries the sign bit for the mantissa while M02 provides the exponent sign. ADDC (Adder Carry) tells the Adder Operation Control when it is necessary to increment the next digit because

of a carry in the present operation. The other four signals, $\overline{N0B1}$, $\overline{N0B2}$, \overline{NTNZ} and $\overline{NT4NZ}$, indicate whether certain bits and nibbles equal zero. They are used by the Entry Register Jump Control to determine the contents of the Entry Register. The Entry Register Jump Control determines the computer's response to conditional jump commands.

The Adder Operation transmits various commands based on the inputs. SOFL (Set Overflow) when high, causes the Instruction Control chip to branch to the Error routine. $\overline{ADD1}$ (Add 1) results from the ADDC signal previously sent to the Adder Control and causes an increment. B Bus determines whether the Input Selector in the Adder/Entry chip selects the parallel Data File output lines or the Serial-to-Parallel Register output as an input to the BCD Adder. CMPL (Complement) is based on a comparison of the sign bits and tells the Adder/Entry to perform a complement operation when required.

2.5.4 ADDER/ENTRY CHIP ACL-06/TCL-06

The Adder/Entry chip contains the Entry Register, input/output selection, BCD Adder and Complement Logic.

The Entry Register is similar to the memory registers, except that it has two additional nibbles, NG (Guard Nibble) and NU (Underflow Nibble) which serve as buffers and indicators of answers outside the range of the computer.

IHTEP is a control for the Parallel-to-Serial and Serial-to-Parallel Registers. Besides acting as converters, these registers provide temporary storage for data being transferred between the Entry Register and Index Register. ILL is a serial input from the Index Register. \overline{SERG} is a serial output for transfer of data from the Entry to the Index Chip.

The Input Selector determines whether the data to the BCD Adder is the parallel Data File output or the Serial-to-Parallel Register output. Similarly, the Output Combiner Selector selects inputs from portions of the Entry Register and determines whether the output goes to the parallel Data File input or to \overline{SERG} .

Normally, the adder operates as a BCD adder, but when BINA (Binary Add) is a logical 1, the BCD Adder becomes a straight binary adder. The Complement Logic, when CMPL is logical 1, converts the digits in the Entry Register to their complements before passing them into the BCD Adder.

2.6 PERIPHERAL SYSTEM CONTROL

Peripheral system control consists of one slide switch, $\overline{\text{INT2}}$, five status bits, and eight flag bits. The slide switch determines whether the content of data or program memory is transmitted to peripheral equipment. The computer determines the current operating mode of the peripheral equipment by the condition of the status bits, and then transmits control information to the peripheral device by software manipulation of Flag Group B. Table 2-4 lists the status and flag bits used for peripheral control, with a brief description of the function of each bit.

Table 2-4
PERIPHERAL CONTROL BIT DEFINITION

Control Bit	Function
$\overline{\text{INL8}}$	Read teletype data
$\overline{\text{INH1}}$	Cassette Drive available
$\overline{\text{INH2}}$	Cassette Drive may accept a computer output
$\overline{\text{INH4}}$	Read cassette data track A
$\overline{\text{INH8}}$	Read cassette data track B
$\overline{\text{INT2}}$	Tells computer to accept data from the Cassette Drive
FBL1	Carries data from the computer to the teletype
FBL2	Teletype punched paper tape motor control
FBL4	Interrupt Enable (Cassette Drive)
FBL8	Cassette Drive Motor control
FBH1	Cassette data track A enable (A1)
FBH2	Cassette data track A enable (A0)
FBH4	Cassette data track B enable (B1)
FBH8	Cassette data track B enable (B0)

Note: $\overline{\text{INT2}}$ and the status signals are inverted to true signals at the chip input.

2.6.1 STATUS CONTROLS

Of the status lines used by peripheral equipment, two lines are interpreted as status, and three lines are interpreted as data by the computer. $\overline{INH1}$ and $\overline{INH2}$ are interpreted as peripheral status by the computer. $\overline{INL8}$, $\overline{INH4}$, and $\overline{INH8}$ are data input lines from the peripheral equipment. Table 2-4 defines those bits.

2.6.2 INTERRUPT CONTROL

The Interrupt 2 channel indicates to the computer when to accept data from the Cassette Drive. The computer WRITES on and READS from the Cassette Drive in 2-bit parallel mode. Four interrupts are generated by the Cassette Drive for each 8-bit byte read from the Cassette Drive, and each interrupt generated causes the computer to branch to the interrupt microprogram. After each interrupt is received by the computer, both $\overline{INH4}$ and $\overline{INH8}$ are considered valid data by the computer.

2.6.3 FLAG GROUP B CONTROL

Flag Group B is used by the computer to control both Cassette Drive and teletype operations. Teletype control includes FBL1 and FBL2 while Cassette Drive control is determined by FBL4, FBL8, FBH1, FBH2, FBH4, and FBH8. Table 2-4 defines those bits.

2.7 DATA FILE PRINCIPLES OF OPERATION

The Data File is the printed circuit board directly beneath the Control board. All Data File boards contain a one ACL-03 or TCL-03 combinational logic chip and three or four read-only memory (ROM) chips. In addition, all Data File boards contain four 1024-bit random-access memory (RAM) chips. Four TTL MSI chips contain the input logic for the RAM memory.

2.7.1 DATA FILE ORGANIZATION AND ADDRESSING

The computer contains 64 columns of memory, numbered octally from 00 to 77. The computer contains provisions for using only columns 40 to 77. Columns 40 through 74 are reserved for

ROMs only; the RAM memory is located in columns 76 and 77. The computer does not use columns 74 and 75.

Each column of memory contains 32 registers. A register may be used as a single data storage register or as a program memory area with a capacity of eight program instructions. All registers contain eight bytes, equal to 16 nibbles or 64 bits. When the register is used for data storage, the nibbles within the register are normally identified decimal numbers 0 through 15. Figure 2-15 shows the structure of a data register.

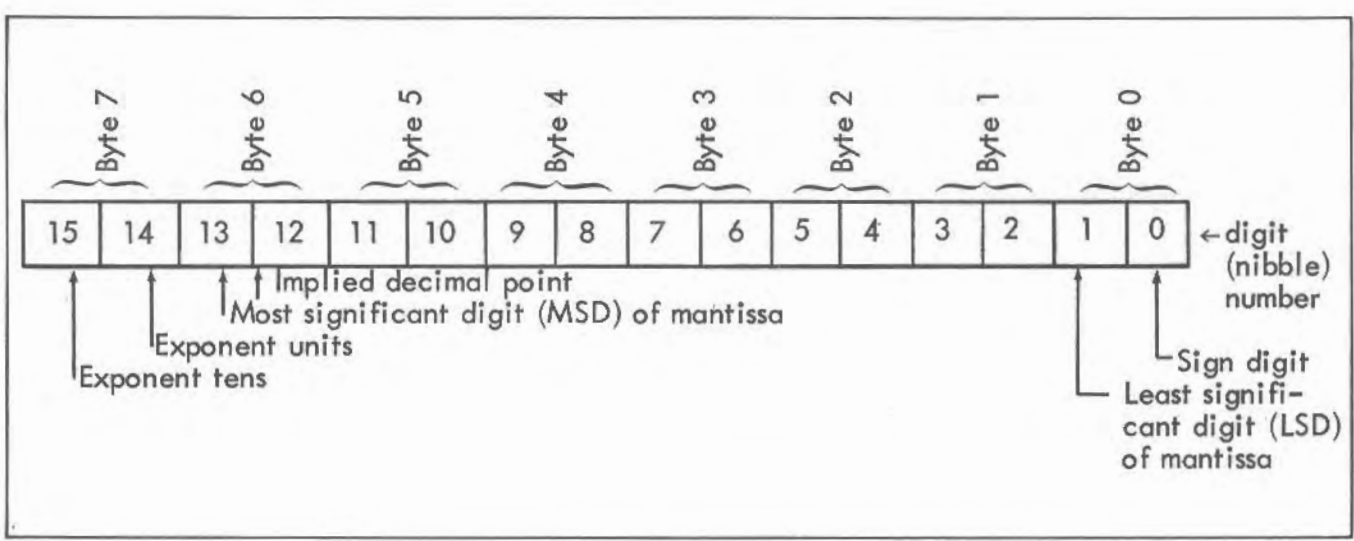


Fig. 2-15 Register Structure

Each decimal digit requires one nibble of storage and one nibble is used for sign information, so each register may contain 15 decimal digits. The computer stores data in exponential form (scientific notation). Thus, each register contains a 13-digit mantissa, a 2-digit power-of-10 exponent, and sign information for both mantissa and exponent. When data is stored in a register, the mantissa has a value between -10 and +10. The exponent may range from -99 to +99.

Internally, the computer addresses the memory in the binary-coded-octal system. When the operator addresses a register, the logic converts the instruction code and keyboard register number into a binary-coded-octal address.

A memory address consists of a 15-bit number as shown in Fig. 2-16. The six most significant bits define the column of memory addressed. The next five bits define the register within the

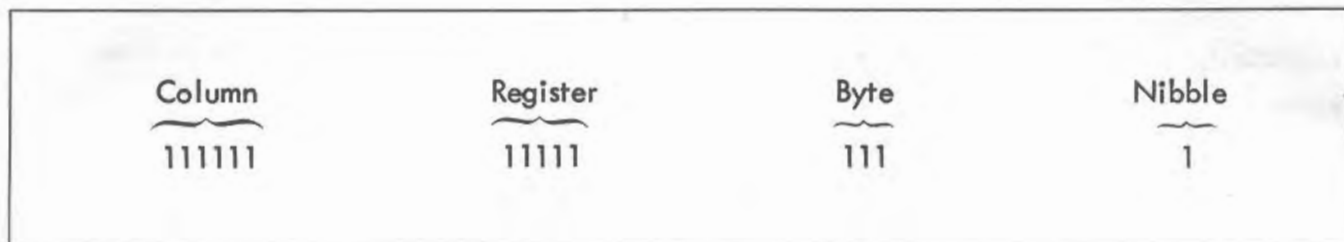


Fig. 2-16 Data File Address Format

column, the next three bits determine a byte within the register and the least significant bit selects the nibble. The address in Fig. 2-16 indicates column 77, register 37, byte 7, nibble 1.

An address is broken down to a specific nibble because data transfers occur along four parallel lines, so the computer transfers four bits, or one nibble, simultaneously. If it is necessary to test or change a specific bit in the memory, the computer transfers an entire byte to the Index Register.

2.7.1.1 Memory Address Chip ACL-03/TCL-03

The Memory Address chip controls the Data File input/output operations. See Fig. 2-17.

The two adders and the adder control circuitry convert instructions (CTRL) and data address inputs ($\overline{\text{DPIN}}$) from Control into addresses usable by the memory.

The program and data pointers contain current program and data addresses. The outputs of these pointers as well as the four signals SC1, SC2, SC4 and SC8 go to the address generator and modifier. The program and data pointers may be exchanged in order to apply the program pointer contents to the address generator and modifier. The address generator provides the write signal (WRIT), the RAM enable signal ($\overline{\text{CTEN}}$) and the address signals A0 through A14.

The signals $\overline{\text{DCIN}}$, $\overline{\text{POOT}}$ and $\overline{\text{DOOT}}$ are used for test only.

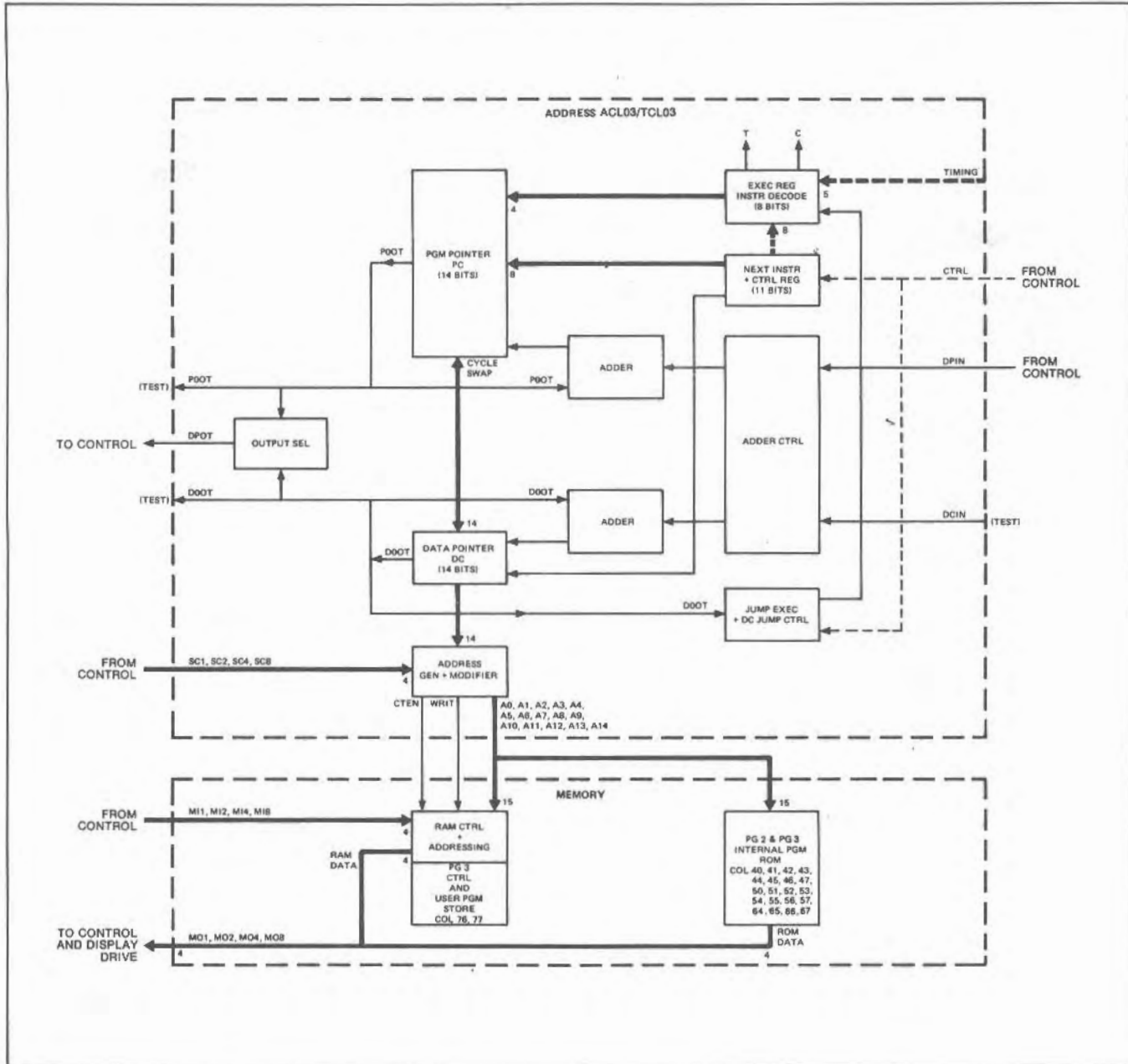


Fig. 2-17 Memory Addressing Functional Block Diagram

2.7.2 ROM MEMORY

The ROM memory contains the microprograms necessary to execute keyboard or program instructions. The ROM memory contains three or four ROM chips, depending on the storage capacity of the ROMs installed. The ROM memory occupies columns 40 through 67 of memory. Table 2-5 identifies the ROMs used and the columns occupied by each ROM.

Table 2-5
ROM USAGE AND COLUMN ASSIGNMENT

Model	ROM	Columns
SCIENTIST	8KR258	40-43
SCIENTIST	8KR079	44-47
SCIENTIST	16KR104 (1)	40-47
SCIENTIST	8KR26A	50-53
SCIENTIST	8KR26B	54-57
SCIENTIST	16KR105 (2)	50-57
SCIENTIST	8KR04D	64-67
SCIENTIST	16KR016 (3) (4)	60-67
SCIENTIST	16KR026 (3) (4)	60-67

(1) The 16KR104 replaces both the 8KR258 and the 8KR079.
 (2) The 16KR105 replaces both the 8KR26A and the 8KR26B.
 (3) The 16KR016 and the 16KR026 are completely interchangeable.
 (4) The 16KR016 and the 16KR026 both replace the 8KR04D.

2.7.2.1 ROM Identification and Usage

The type designator on each ROM chip identifies the size, application and location in memory of the chip. The following example uses an 8KR26A.

The 8KR identifies the chip as an 8192-bit ROM containing 1024 micro-instructions. An 8K ROM occupies four columns of memory.

The 26 means that the chip is the 26th 8K "A" ROM designed for use in this general equipment series. The final character (A) identifies the location of the chip in the memory organization. The combined designator 26A identifies the chip application.

The 16K ROM chips are similar to the 8K ROMs; the most significant difference is that the 16K ROM series contains twice as many micro-instructions as the 8K ROMs. The ROMs may be either 16KR or 16KN types. The 16KR ROMs use P-channel field-effect transistors while the 16KN ROMs use N-channel field-effect transistors. These internal differences result in a different value of supply voltage; otherwise, the circuits external to the chip are identical for both types.

2.7.2.2 8K ROM Functional Description

All 8K ROMs function in the same manner; the only differences among the types are the micro-instructions stored in the matrix and the programmed connections for the chip select logic. Refer to Fig. 2-18 for the following description.

The ROM requires three supply voltages: V_{SS} , V_{DD} and V_{GG} . These voltages are applied to pins 1, 28 and 19, respectively. The clocks $\Phi 1$ and ΦR are applied to pins 2 and 3 for internal timing.

The 15 address lines, A0 through A14, are applied as shown in Fig. 2-18. The logic levels present at A11 through A14 determine whether a particular ROM is to be activated. If the ROM shown were an 8KR258, the output of the chip select logic would be logical 1 only when A14 is a logical 1 and A11, A12 and A13 are logical 0. Address lines A9 and A10 operate in conjunction with the quadrant enable gates to select one quadrant of the storage matrix.

The quadrant enable pins, Q0E through Q3E, are not connected externally in normal operation and are held at a logical 0 by V_{DD} applied through the internal resistor. When a logical 1 is applied to one of these pins, that quadrant of the ROM is disabled. When substitute ROMs are piggy-backed, the adapter clip applies a logical 1 to these four pins, disabling the original ROM.

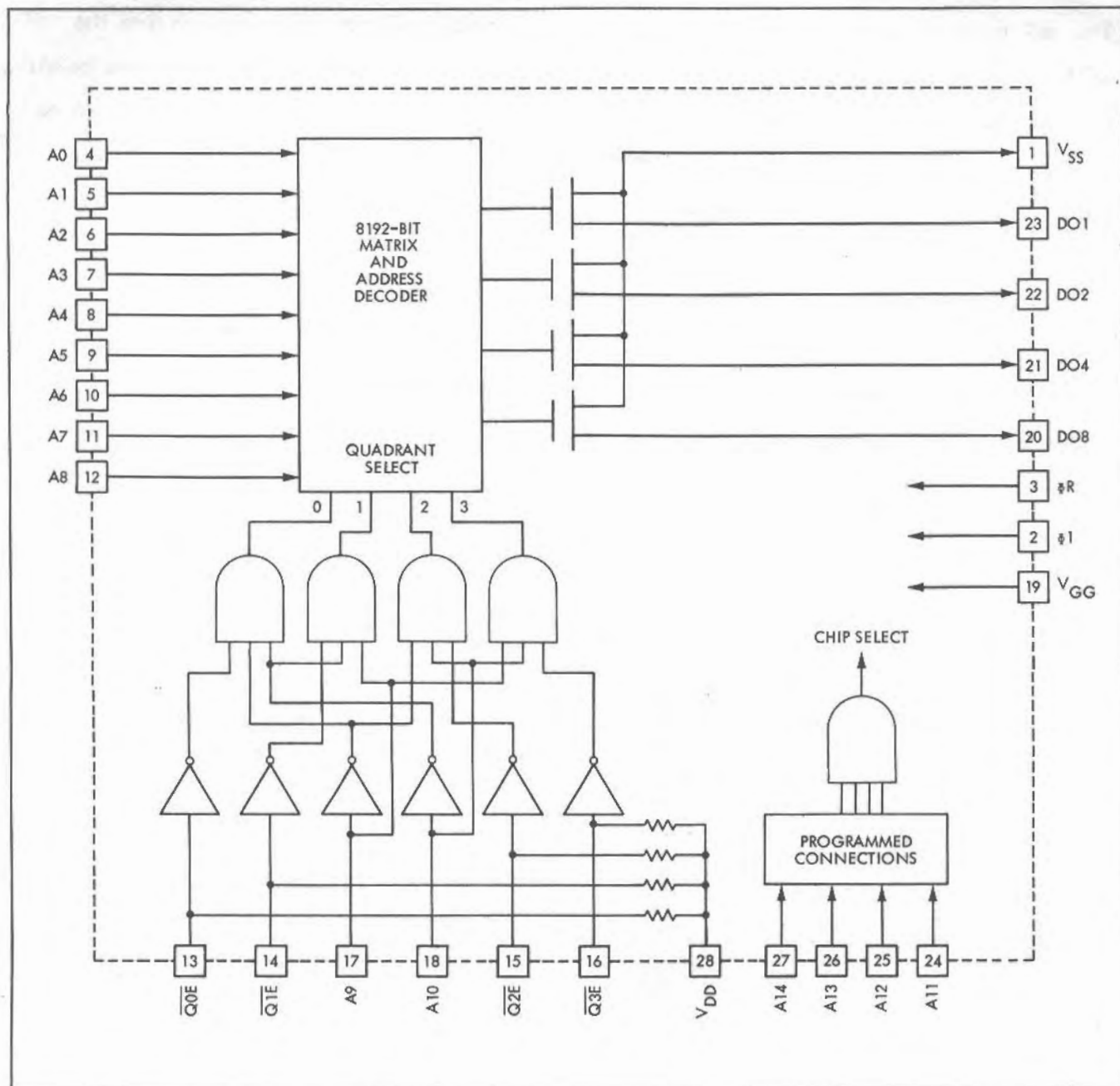


Fig. 2-18 8K ROM Functional Block Diagram

Address signals A0 through A8 select the specific nibble to be read from the ROM. Those output bits which are logical 1 turn on the field effect transistor output buffers, coupling V_{SS} to the output lines. Any FET not turned on presents a very high impedance between the output line and V_{SS} . Since the output lines are coupled to V_{DD} through resistors external to the ROM, several output lines may be paralleled without shunt impedances causing false logic levels. The ROM output appears on lines D01, D02, D04, and D08 to the common data bus M01, M02, M04, and M08. The data bus is described by Par. 2.7.2.4.

2.7.2.3 16 K ROM Functional Description

The 16KR and 16KN ROMs are logically identical, the only difference being the field-effect transistors used by the two series. The variation affects the external circuitry only in that the 16KN ROM requires V_{DD} at pin 19 rather than V_{GG} as shown in Fig. 2-19.

The ROM requires three supply voltages: V_{SS} , V_{DD} and V_{GG} . These voltages are applied to pins 1, 28, and 19, respectively. Clocks $\Phi 1$ and ΦR are applied at pins 2 and 3 for internal timing.

The 15 address lines, A0 through A14, are applied as shown in Fig. 2-19. The logic levels at A12 through A14 determine whether a specific ROM is activated. If the ROM is a 16KR114, it is selected only when A14 is at logic 1 and A12 and A13 are at logic 0. Address lines A10 and A11 operate in conjunction with the quadrant enable gates to select one quadrant of the storage matrix.

The quadrant enable pins, $\overline{Q0E}$ through $\overline{Q3E}$, are usually unconnected and held at logic 0 by V_{GG} applied through the internal resistors. When a logical 1 is applied to one of these pins, the corresponding quadrant is disabled. When used to piggy-back substitute ROMs for troubleshooting, the adapter clip applied logic 1 to these four pins, disabling the original ROM.

Address lines A0 through A9 select the nibble to be read. Output bits which are logical 1's turn on the field-effect transistor output buffers, coupling V_{SS} to the output lines. A FET not turned on presents a very high impedance between the output line and V_{SS} . External resistors bias the off outputs to V_{DD} , preventing the transistor cutoff current from causing false output levels.

The ROM output on lines D01, D02, D04, and D08 go to the common data bus M01, M02, M04, and M08. The data bus is described in Par. 2.7.2.4.

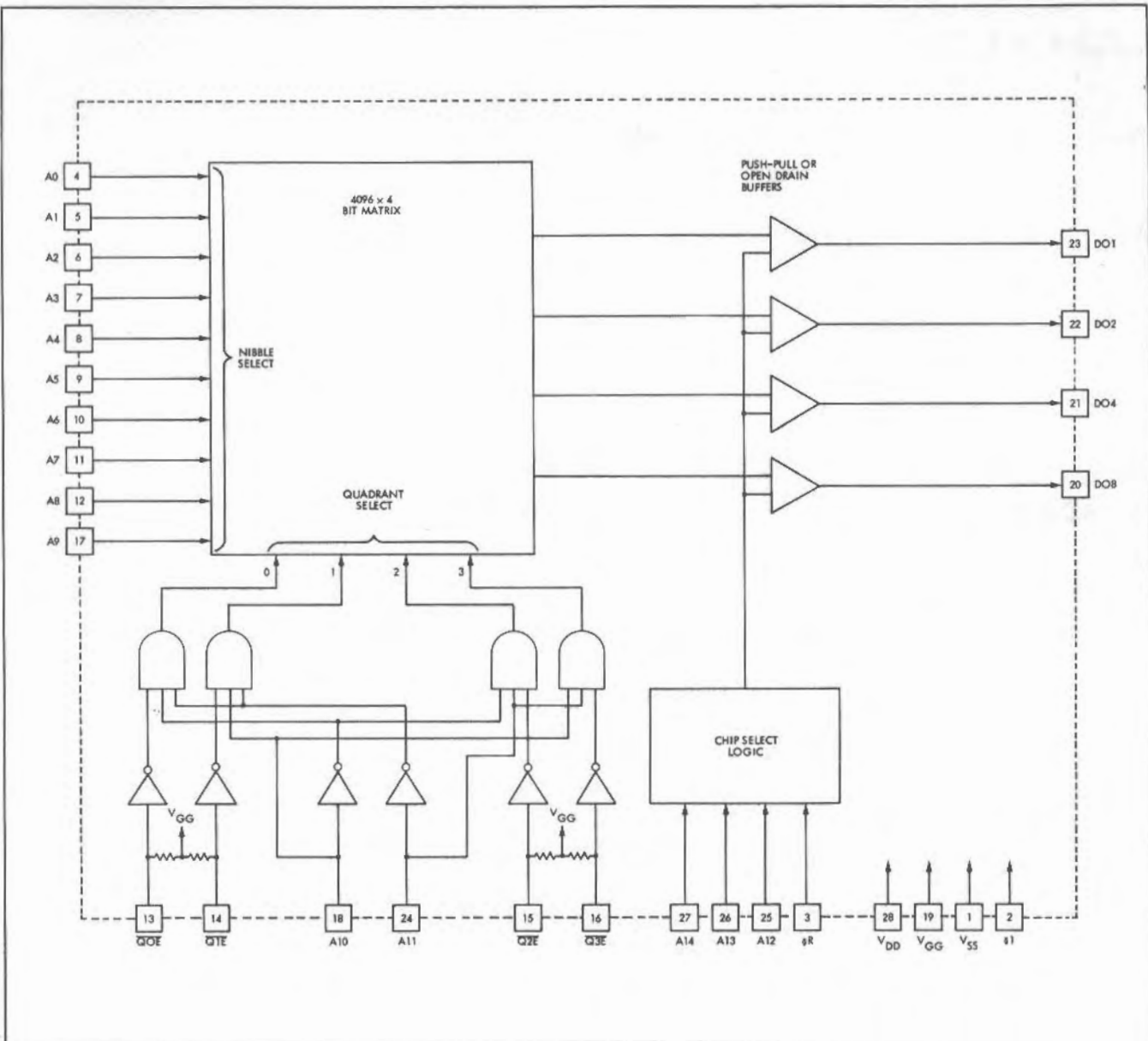


Fig. 2-19 16K ROM Functional Block Diagram

2.7.2.4 ROM Data Path Functional Description

The ROM outputs are carried by D01, D02, D04, and D08 to transistors Q4, Q3, Q2, and Q1, respectively. The transistors are connected in the common emitter configuration. All lines operate in the same manner, so the circuit associated with Q1 and D08 is discussed. Refer to Fig. 2-20 for the following discussion.

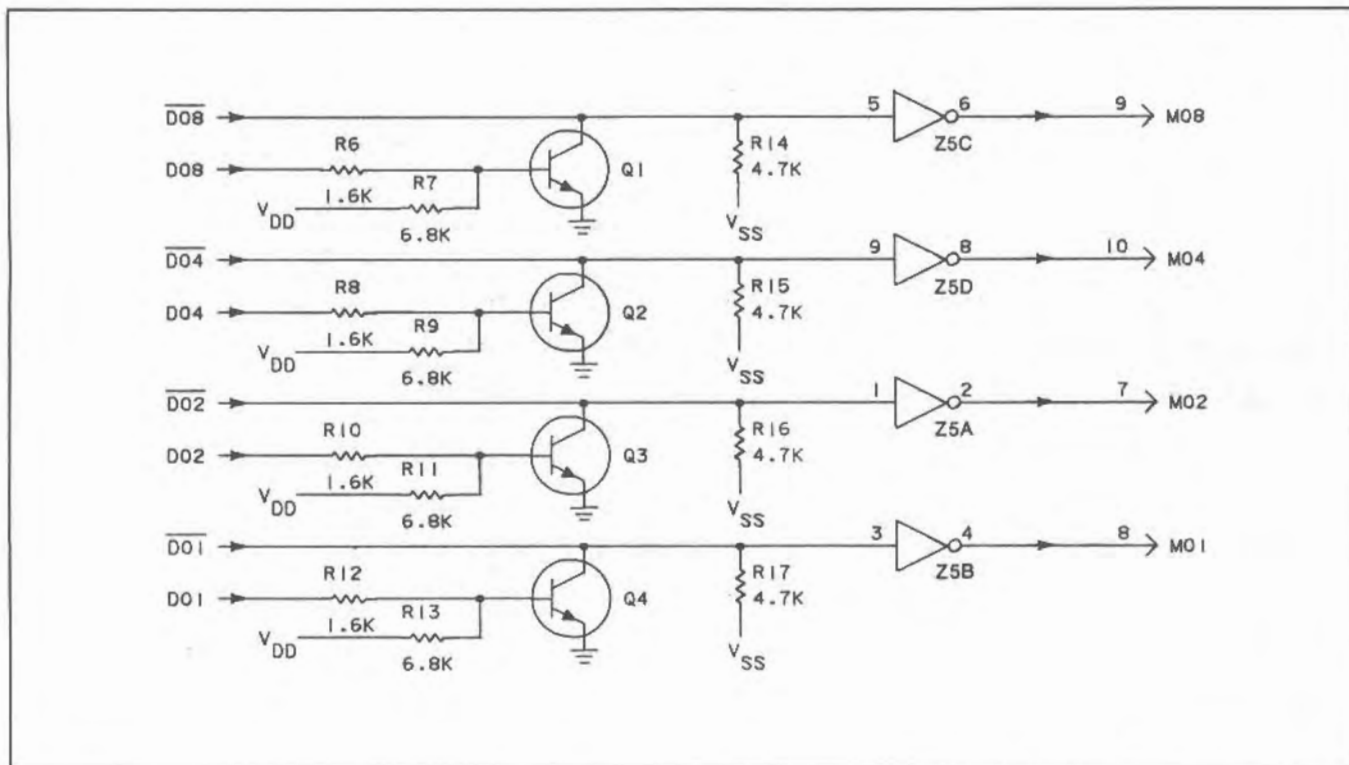


Fig. 2-20 Memory Output Lines

The common emitter circuit acts as an inverter. When D08 is a logical 1, Q1 turns on which shorts the V_{SS} level across R14 to ground. Z5C sees V_{DD} or a logical 0 at the input, and transmits a logical 1 on line M08.

When D08 is a logical 0, Q1 sees V_{DD} on its base, which cuts Q1 off. Z5C sees the V_{SS} across R14, or a logical 1, and Z5C transmits a logical 0 on line M08.

$\overline{D01}$, $\overline{D02}$, $\overline{D04}$, and $\overline{D08}$ are outputs from the RAMs. The data line operations for RAM data is discussed in Par. 2.7.3.2.

2.7.3 RAM MEMORY

The RAM memory contains the keyboard storage registers, the user program memory and the computer working storage. The RAM memory consists of four 1K RAM chips and four MSI chips which adjust the timing and act as input buffers. The RAMs occupy columns 76 and 77 of the memory.

2.7.3.1 1K RAM Functional Description

The RAMs used in the computer are static type 2102 or 2602 1024-bit RAMs. See Fig. 2-21.

Each chip contains a storage matrix arranged in 32 rows and 32 columns. To perform either a read or write operation, the chip must have a logical 0 applied to pin 13 (\overline{CE}). The READ/WRITE signal applied to pin 3 determines whether the chip will read from or write into the RAMs. A logical 1 at pin 3 indicates a read command, while logical 0 is a write command.

During a write operation, the data enters at pin 11. Data leaves the chip at pin 12 during a read operation.

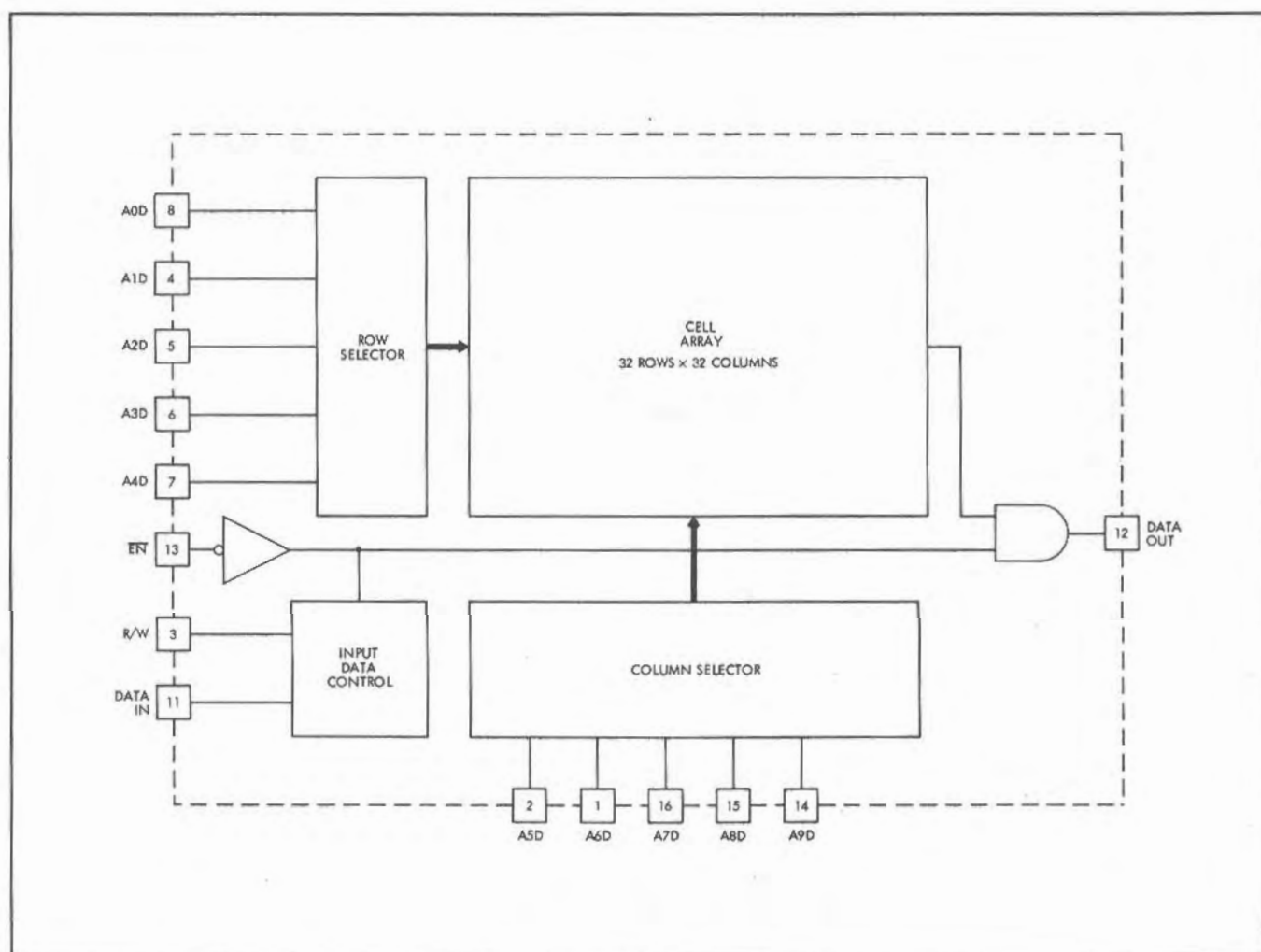


Fig. 2-21 1024-bit RAM Functional Block Diagram (National Type 2102)

Memory address signals A0D through A4D define a row within the matrix. A5D through A9D define the column. The intersection of a row and column selects the specific cell to be read or written.

2.7.3.2 RAM Data Path Functional Description

When writing data into the RAMs, Control applies the memory input to pins 2, 3, 6, and 7 of a 4-bit latching register, Z10, via lines M11, M12, M14, and M18 (Fig. 2-22). The IC, Z10, gates the input data to the outputs when the clock input is a logical 1. When the clock input goes to a logical 0, the outputs remain latched to the input levels present at the time of the clock transition. The complementary outputs apply data to the RAMs. The logic levels at the RAM inputs are the complement of M11, M12, M14, and M18.

When clock $\Phi 2$ goes to a logical 0 at the center of the bit time, the register latches to the logic levels present during the first half of the bit time, and remain in that condition until the beginning of the next bit time. The write signal is not applied to the RAMs until the second half of the bit time to assure stable input logic levels when writing.

Refer to Figure 2-20 for the following discussion. During the Read operation, data passes from the RAMs by lines $\overline{D01}$, $\overline{D02}$, $\overline{D04}$, and $\overline{D08}$ to inverters Z5B, Z5A, Z5D, and Z5C, respectively. The inverters complement the RAM output levels to "true" data, and transmit the data on lines M01, M02, M04, and M08 to the area of the computer specified by the Control.

2.7.3.3 RAM Control

The Memory Address chip generates the address and control signals used by the RAMs. Whenever the computer performs an operation requiring access to the RAMs, the Memory Address chip generates the RAM enabling signal, \overline{CTEN} , and the address signals A0 through A9.

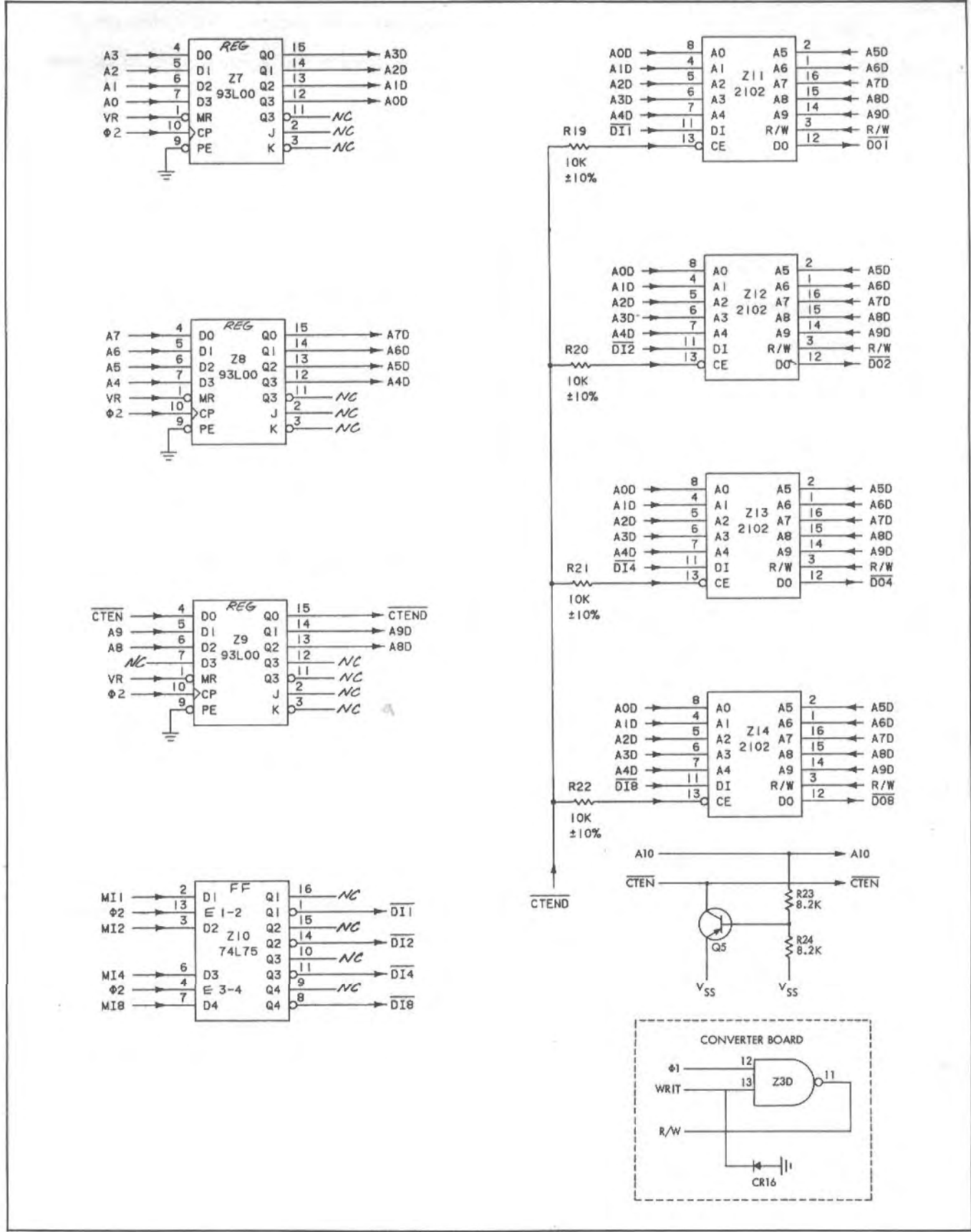


Fig. 2-22. RAM Memory Input/Output Schematic Diagram

For a read operation, the ACL-03/TCL-03 applies \overline{CTEN} and the addresses to Z8, Z10 and Z12. These chips are 4-bit serial/parallel shift registers connected to operate as parallel registers only. The registers transfer the data on positive-going transitions of the clock at pin 10. $\Phi 1$ is the clock for the registers, so the transfer occurs when $\Phi 1$ makes a negative transition, just prior to the end of the bit period. Therefore, the address and enabling signals applied to the registers will actually enable the RAMs in the next bit time; when the Control uses the data.

For the write operation, the Memory Address chip sets up the addresses and enable signal as for the read operation. During the next bit period, it transmits the WRIT signal to the Converter board, where WRIT is NANDed with $\Phi 1$ to generate R/W, the READ/WRITE signal. During the second bit period, the RAMs see the address and enabling signals transmitted from the Memory Address chip during the first bit period and, in the last half of the second period, R/W goes to logic 0. The RAMs then write into memory the data transmitted from Control during the first half of the second period. $\Phi 1$ returns to a logical 0, terminating the write command, at the same time that $\overline{\Phi 1}$ goes to logical 1 and shifts in a new address.

When RAM memory is addressed by Control, only columns 76 and 77 are available, and A10 is a logical 1. Should A10 go to a logical 0, as it would for the columns 74 and 75, Q5 would turn on, pulling \overline{CTEN} to V_{SS} , disabling the RAM enable signal.

2.8 COMPUTER TIMING

The basic time unit for instruction execution is the machine cycle, consisting of 20-bit times, designated T0 through T19 as shown in Fig. 2-23. Control generates the timing signals C01P through C16P. The computer uses these signals to perform functions during a specific bit time within the cycle. In general, the computer executes a single instruction each machine cycle or a double instruction (Branch, Jump, etc.) in two cycles.

2.8.1 MACHINE CLOCKS

The ACL-07/TCL-07 on the Control board generates the clocks used to define a bit time within the cycle. The name of each clock signal identifies the bit weight; e.g., C08P has a bit weight of eight when it is logical 1. The P at the end of the signal name means that the signal is

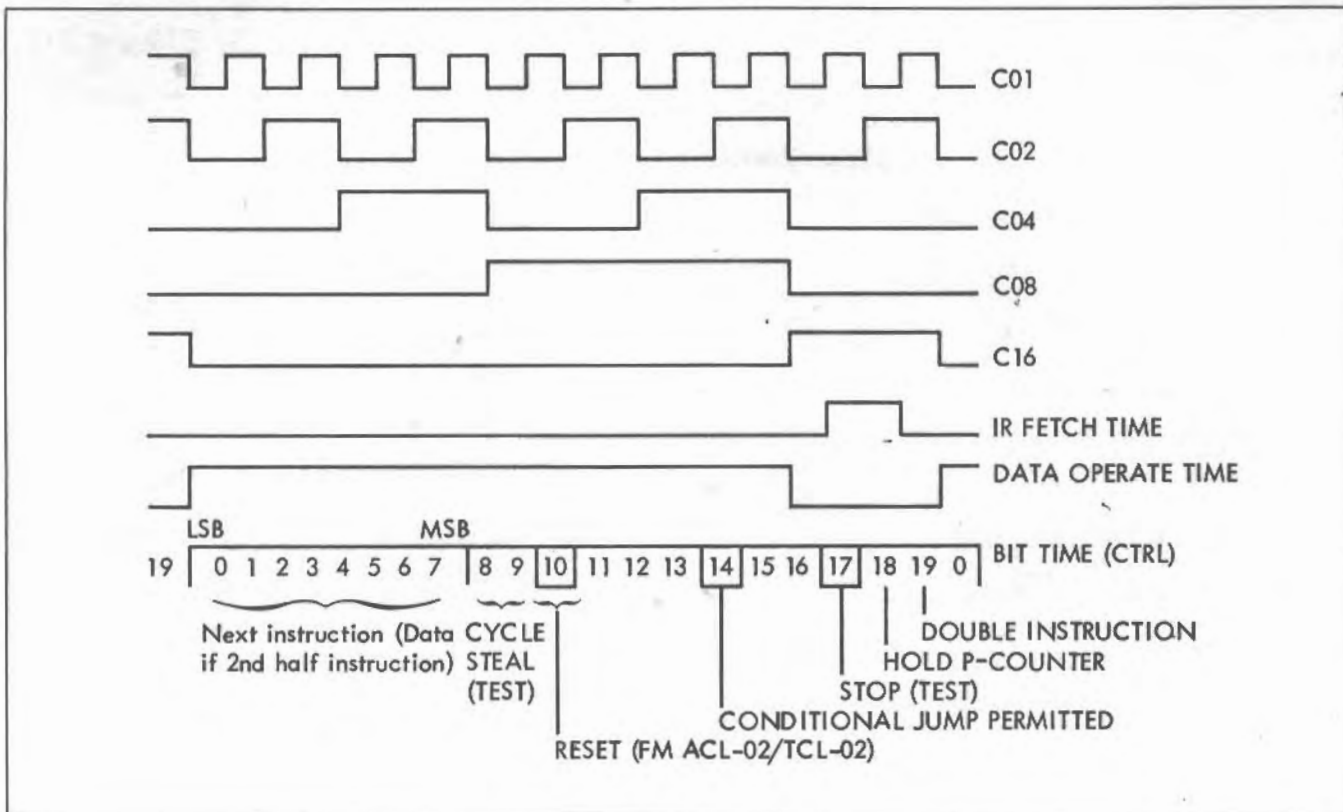


Fig. 2-23 System Timing

actually generated and transmitted one bit-time ahead of its true time; however, since most other signals are also advanced by one bit-time, the signals may be considered present at their true time when making oscilloscope observations.

2.8.2 INSTRUCTION TIMING

Instructions for the combinational logic chips are generated in the Instruction Control chip, ACL-04/TCL-04. The Instruction Control chip assembles the control instruction during times T16 through T19 of a cycle. During times T0 through T7 of the next cycle, it distributes the instruction to the system via CTRL, where it shifts serially into the Next Instruction Registers of the MOS/LSI chips. At T16 or T17 the chips transfer the instruction in parallel to the Execution Registers. The chips execute the instruction during the following 20-bit times.

The Instruction Control chip identifies double instructions by transmitting a 1 during T19 of the cycle in which the first of the double instruction is distributed. The logic in the MOS/LSI chips

recognizes that the second half of the instruction will arrive in the next cycle and waits for it. The second half of a double instruction is either an address for branches and jumps or a number to modify the Index or DC Registers.

During T8 to T18 the CTRL line carries other signals used to modify operation between instructions. The bits of T8 and T9 are cycle steal signals used by the factory test equipment. The T10 bit is a Reset pulse generated by the Keyscanner chip. The bit at T14 indicates whether a conditional jump is permissible. The T18 bit is used to stop the computer during automatic test. The T18 pulse stops the P-Counter while executing certain instructions. It also allows the automatic test equipment to operate the logic in a single-step mode.

2.8.3 DATA FILE TIMING

During a RAM memory operation, the computer may write into or read out the memory 1 nibble for each bit period during the RAM operate time. If the RAM data is coming from a serial-to-parallel converter or going to a parallel-to-serial converter, Control enables the RAM memory only at every fourth bit time to allow for the delay in conversion.

Within the machine cycle, the period T0 through T15 is reserved for RAM memory operations, while the ROMs are read during T17 and T18. Control transmits addresses A0 through A14 and the RAM enable signal, \overline{CTEN} , 1 bit ahead of the actual operate time. WRIT and the memory input data occur at the true bit time.

The computer addresses the ROMs during T17 through T18. The ROMs output one nibble during each of the two periods T17 and T18, allowing one micro-instruction to be read each cycle.

2.9 EXAMPLES OF OPERATION

The following examples partially describe the way the computer performs selected operations. The abbreviated descriptions are intended to convey only a general concept manner in which the computer executes commands.

2.9.1 KEY DECODE

When the operator depresses a key, the Keyscanner encodes the switch closure and, as a result of the READ KEY instruction, transmits it to the Index Register via IXDI, as described in Par. 2.3.3. When the key code has loaded into the Index Register, the computer branches to the Key Decode routine. This routine consists of a decision "tree" in which each bit of the Index Register is checked in sequence. See Fig. 2-24. The instruction following the check of the last bit will be a Branch instruction in which the address portion represents the first step of the routine executing the function represented by the key.

2.9.2 NUMERAL ENTRY

Numeral Entry includes entering the numeric digits, the decimal point, the exponent, and changing the sign. The computer uses the four subroutines described below. The description of these subroutines is for the following key sequence: 1, Decimal Point, 2, CHG SIGN, EXP, 1, 1.

2.9.2.1 Initial Numeral Entry

The Numeral Entry routine controls the entry of numerals into the correct digit position of the Entry Register. Refer to the flowchart, Fig. 2-25.

When the operator presses the 1 key, the computer goes through the Key Decode routine previously described and jumps to the Numeral Entry routine. The key code is still in the index register, so Control first transfers Index Low (IL) to Index Store (IS) to save the numeral. The numeral entry codes contain all zeros except in the four least significant bits, which were in IL, so all necessary bits will be retained.

Next, the computer transfers the contents of I4, a portion of column 77 used for indexing numeral entry status, to the Index Register. Since this is the start of a new entry, all bits are 0. The computer tests the bits now in the Index to determine the type of entry (new entry, continuation of entry, integer, decimal, exponent).

The first bit checked is IL bit 1, which tells whether this is a new entry or a continued entry. IL1 is 0, indicating the start of a new entry, so the routine jumps to the left in the flow chart.

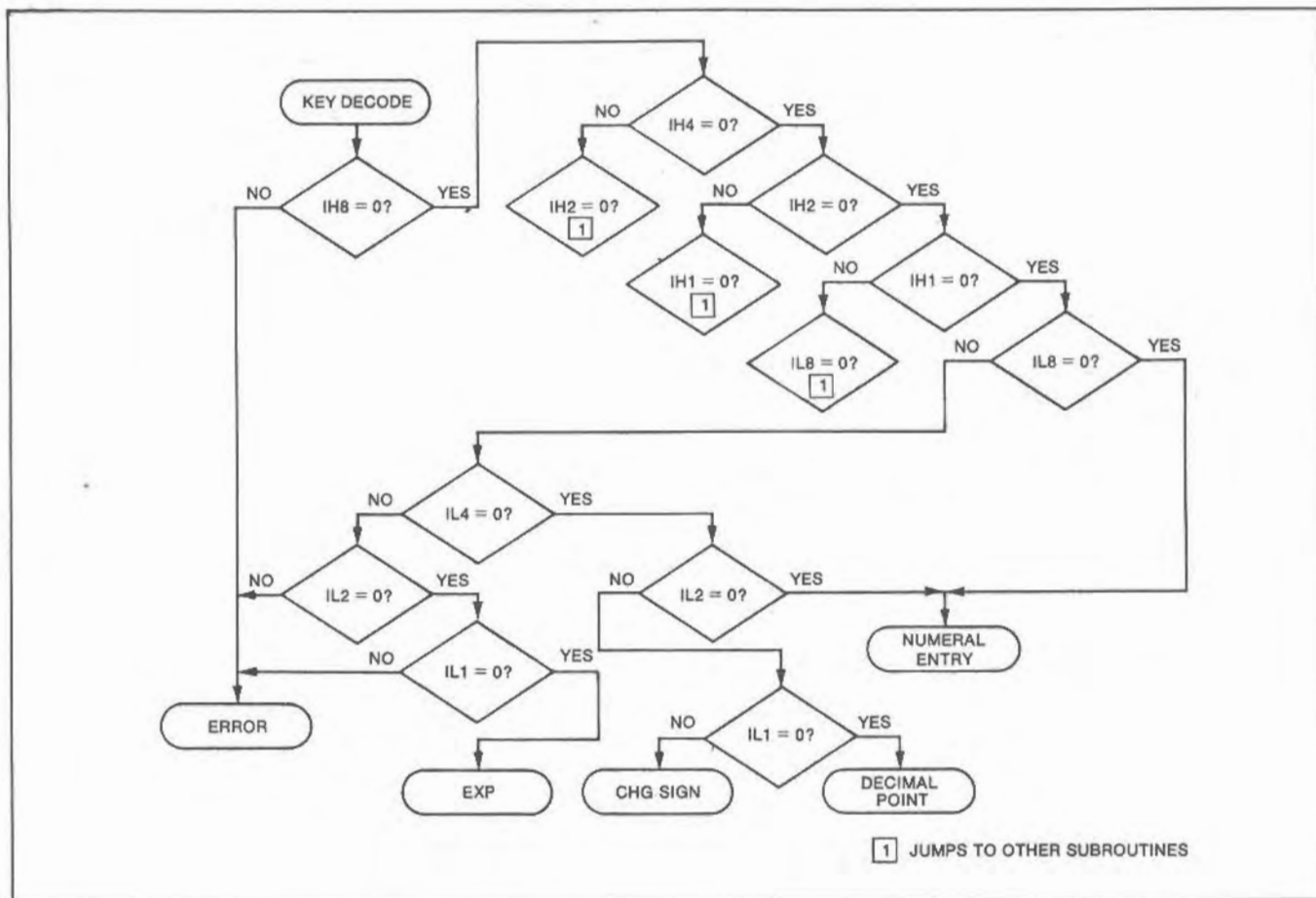


Fig. 2-24 Key Decode Partial Flow Chart

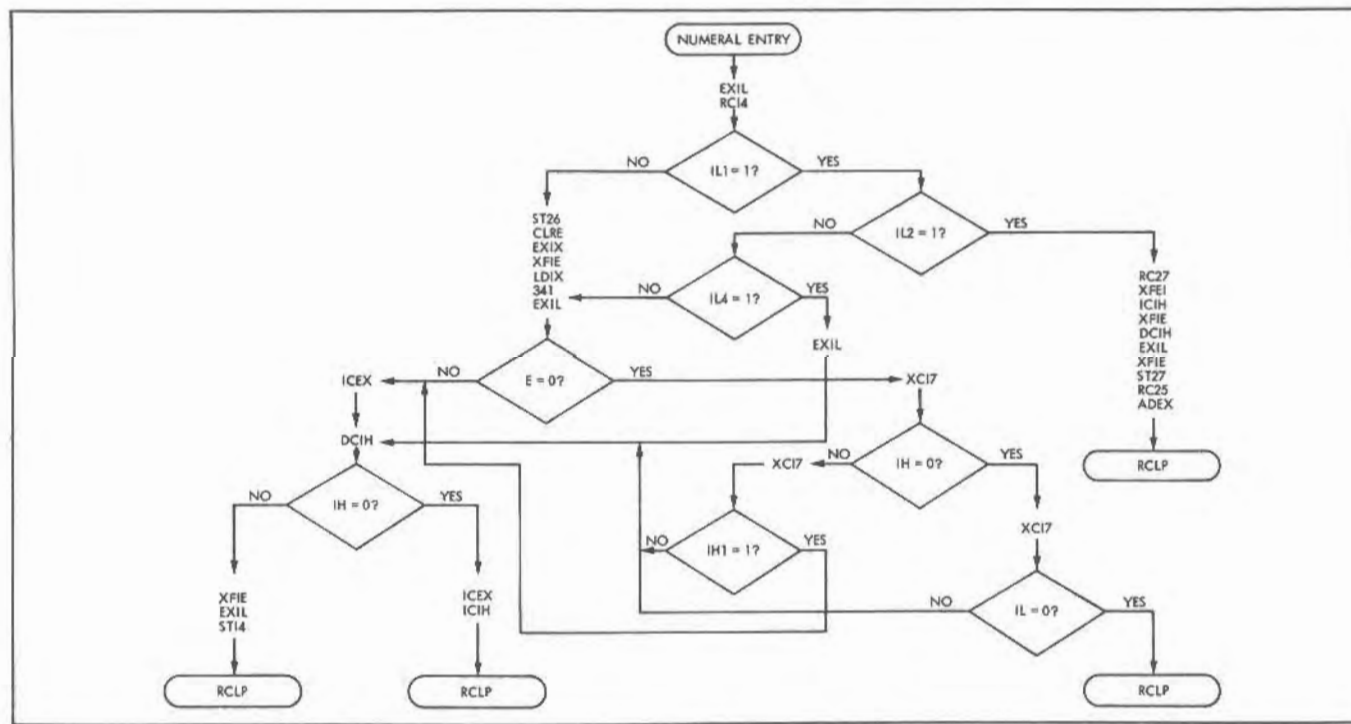


Fig. 2-25 Numeral Entry Flow Chart

The computer stores the contents of the Entry Register in column 77, register 26, and clears the entry. Then, it exchanges IH with IL, and transfers the contents of IL to the digit position of the entry indicated by IH. For this digit entry, IH and IL are filled with zeros, so the entry remains clear. The computer loads the index with the octal number 341 (binary 11100001) and exchanges IL with IS, returning the numeral to IL.

The computer checks if the entry is 0, which it is, so the program jumps to the right. Next, it exchanges the Index with I7, another index register in column 77, and checks to see if IH equals 0. I7 is where the key code was stored during the Key Decode routine, so IH is 0 and the flow continues out the right side of the box.

The computer re-exchanges the Index with I7 and checks if IL is 0. A 0 in IL at this point would mean that the first numeral was 0 and the computer would return to the Idle routine. Since IL is 1, the program jumps to the left from the decision box.

The computer decrements IH, reducing its value to 1101 (decimal 13), representing the most significant digit position. Next it checks to see if IH is 0. Zero in IH would indicate the 14th digit entry and result in an exponent increment. Since IH does not equal 0, the program follows the path to the left of the decision box.

The numeral in IL (0001 or decimal 1) transfers to the Entry Register at the digit position indicated by IH (1101, digit position 13). IL is again exchanged with IS.

The entry now contains the first numeral (1) in the proper digit position and the Index contains the updated numeral entry information. IH shows the digit position of the latest entry, while IL has a one in the IL1 position to indicate that numeral entry is in process. This updated numeral entry information is stored in I4 to be used for the next digit. The computer then returns to the Idle routine.

2.9.2.3 Decimal Point Entry

When the operator presses the Decimal Point Key, the key decode routine places the computer in the Decimal Point routine. See Fig. 2-26. The first instruction is to recall I4 to check the numeral entry status. The computer checks bit IL1. IL1 is 1, so the program jumps to the right and checks the contents of the Entry Register. The entry is not 0 because the operator has already entered a 1, so the program jumps to the left. The next instruction, a double instruction, ORs

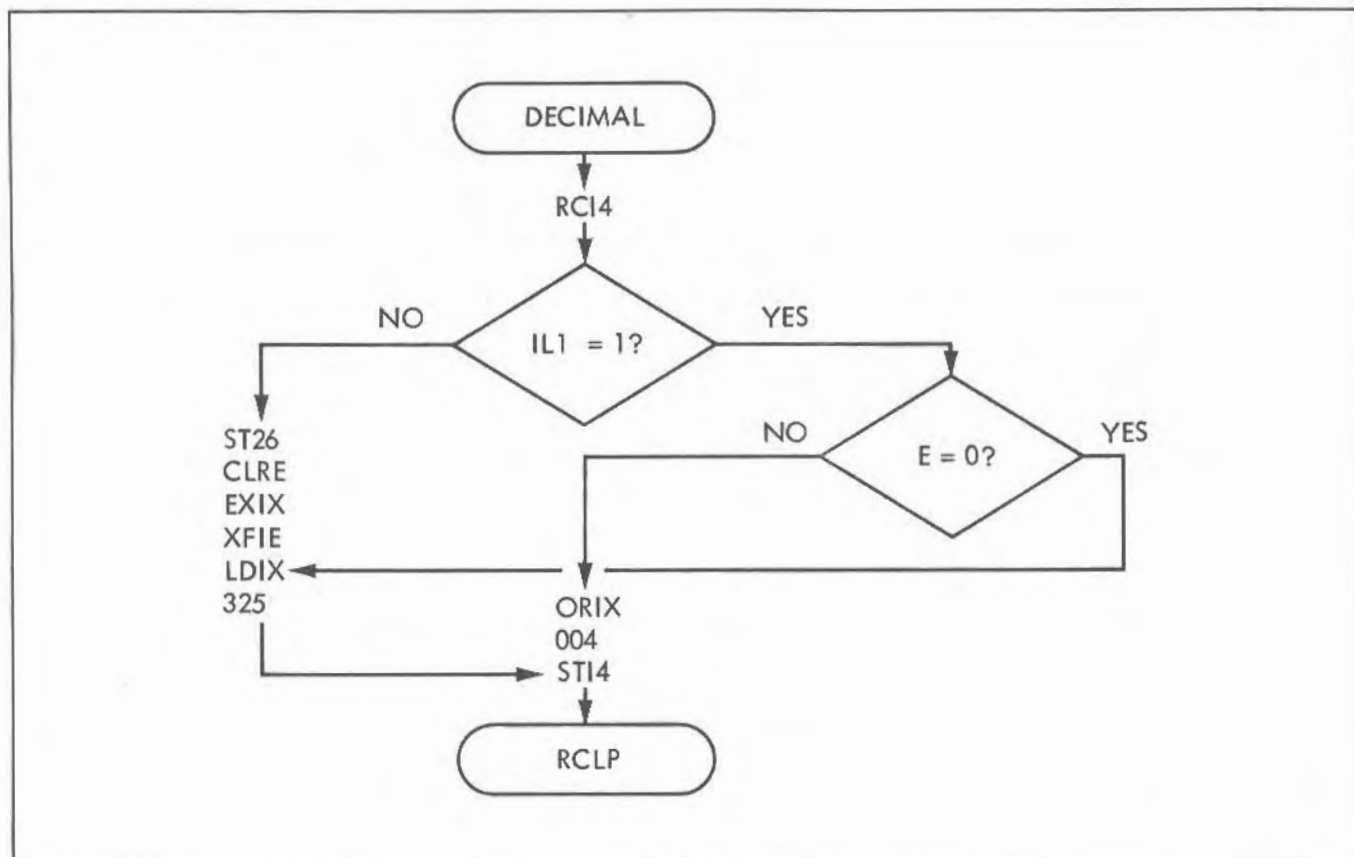


Fig. 2-26 Decimal Point Flow Chart

the Index Register with the octal number 004 (binary 00000100). I4 at the beginning of the routine was 11010001; this has been converted in the Index to 11010101. The computer stores this updated numeral entry information in I4 and returns to the Idle routine.

If the Entry Register had been 0, indicating that the decimal preceded numeral entry, the flow would have been out the right side of the "E=0"? decision box. The computer would have loaded the index with the octal number 325 (binary 11010101). The contents of IH would be 1101, pointing to digit position 13; the first numeral entered would then go into digit position 12. IL would be 0101, indicating that a numeral entry sequence had begun (IL1) and that the decimal had been entered (IL4). The new status information would have then been stored in I4 for use during subsequent entries.

On the other hand, if, at the start of the routine, IL1 had been 0, indicating the start of a new numeral entry, the computer would have stored the entry in column 77, register 26, and cleared the entry. Then it would have loaded the index with the octal code 325 as described above and stored this value in I4 as updated numeral entry information before returning to the Idle routine.

2.9.2.3 Numeral Entry After Decimal

When the operator presses the 2 key, the computer again branches to the Numeral Entry routine (Fig. 2-25). Again, it exchanges IL with IS to save the numeral and recalls 14. As in the first entry, it checks IL1. The Numeral Entry routine previously executed set the bit to a 1, so the flow is out the right side of the decision box and the computer checks bit IL2, which tells the computer if the EXP key has been pressed. The operator has not yet made an exponent entry, so this bit is 0 and the flow continues out the left side of the decision box to the next decision operation, where it checks the status of bit IL4.

IL4 tells the computer if the Decimal Point key has been pressed. Since the operator has pressed Decimal Point, IL4 is 1. The program jumps to the right of the decision box and re-exchanges IL with IS, placing the two back in the Index. Next, Index High is decremented. It was 1101; now it is 1100, pointing to digit position 12. Now the computer checks to see if IH equals 0, a condition indicating that the operator has attempted to enter 14 digits in the mantissa. Since IH is not 0, the flow is to the left from the box. The computer transfers the 2 in IL to digit position 12 as pointed by IH. IL is exchanged with IS to reassemble the numeral entry status information in the Index. The Index is stored in 14 and the computer returns to the Idle loop.

2.9.2.4 Change Sign

As in Numeral Entry, the first action of the Change Sign routine is to recall 14 and determine numeral entry status. See Fig. 2-27.

Again, IL1 is checked first; it is 1, so the program flow continues to the right and checks IL2. The operator has not pressed the exponent key, so IL2 is 0. Program flow continues from the left of the decision box. The computer is no longer concerned with the numeral entry status, so it clears the Index and performs an XFEI operation, in which the digit position of the entry indicated by IH is transferred to IL. Since the Index was cleared, IH points to digit position 0, the sign nibble. Next, the computer performs an Exclusive OR on the Index with the octal number 001 (binary 00000001). Exclusive OR causes IL1 to reverse. Finally, IL is transferred back to the entry at digit position 0. Bit 1 of digit 0 is the mantissa sign bit, which has been changed to 1, making the mantissa negative.

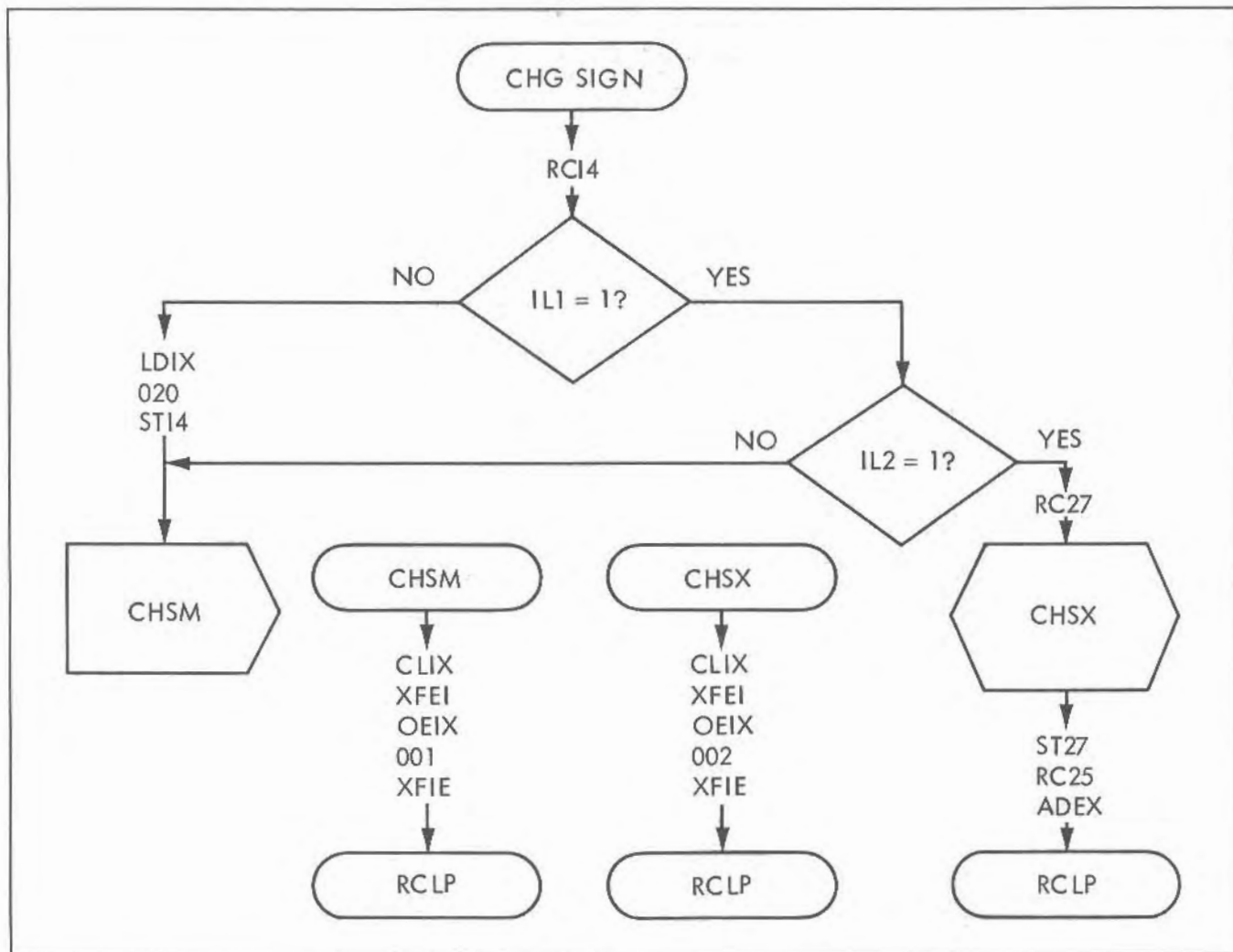


Fig. 2-27 Change Sign Flow Chart

2.9.2.5 Exponent Entry

Figure 2-28 shows the action taken when the operator presses the EXP key. The computer recalls 14 to the Index and checks IL1. This is a continuation of a numeral entry; IL1 equals 1 and program flow continues to the right from the decision box. Next, the status of the Entry Register is checked. The entry contains -1.2, so the program branches left to Justify.

Justify is a separate routine used by most key functions. The routine places the number in the entry into correct exponential form, with a mantissa equal to or greater than 1 but less than 10. The computer temporarily stores the justified number in column 77, register 25, then clears the Entry Register. Next, it stores the entry in column 77, register 27, clearing register 27. When the operator enters the exponent numerals, the computer will use register 25 to store the mantissa and register 27 to store the exponent.

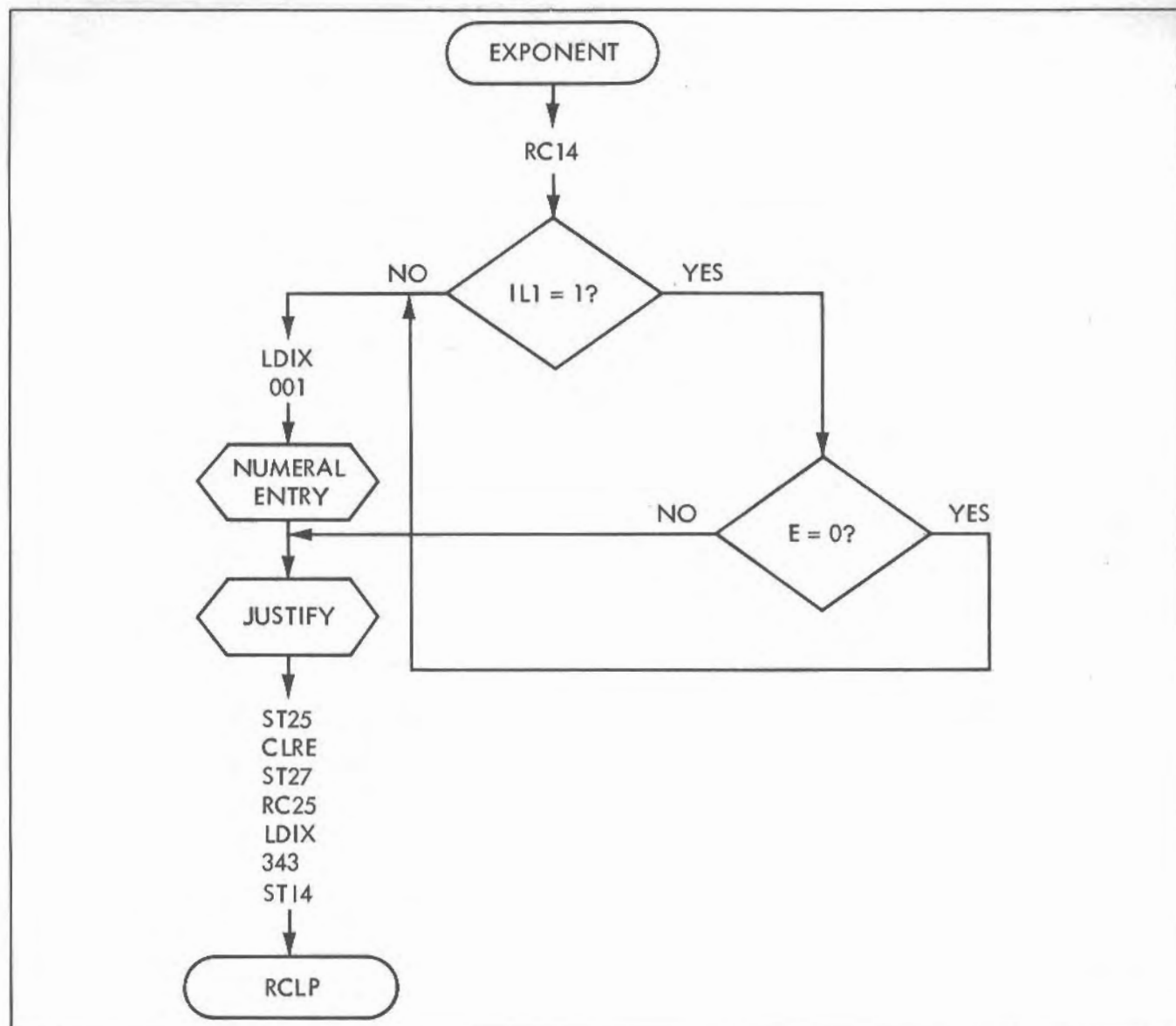


Fig. 2-28 Exponent Routine Flow Chart

Register 25 is recalled to the entry. The computer loads the Index with the octal number 343 (binary 11100011) and stores this value in I4 (updated numeral entry information).

If the EXP key had been the first step in entering a number (or if all mantissa entries had been 0), the computer would have loaded the Index with octal 001 and branched to the Numeral Entry routine to set the mantissa to 1. After executing Numeral Entry, it would have continued from Justify as described above.

To follow the process of entering exponent digits, refer again to the Numeral Entry flow chart, Fig. 2-25. When the operator presses the one key after EXP, the process will be the same as

for mantissa entries until the program checks IL2. For mantissa entries, IL2 is 0; the Exponent routine has set the bit to 1, so the program flow is to the right of the decision box.

The computer recalls register 27 to the entry (sets the entry to 0) and transfers digit 14 from the entry to IL. Index High is incremented to point to digit 15. The computer transfers IL to digit 15 of the entry and decrements IH to again point to digit 14. It then exchanges IL with IS, bringing the exponent numeral back to IL, and transfers the numeral to digit position 14 (exponent units digit). The new value of the entry is stored in column 77, register 27, and column 77, register 25 is recalled to the entry.

The entry now contains the mantissa, while the exponent is stored in register 27. The final instruction adds the exponent of register 27 (01) to the exponent of the entry (00). The entry now contains a mantissa of -1.2 and an exponent of 01. The computer returns to the Idle routine.

When the operator presses the second numeric key for the exponent, the same routine is executed. The computer recalls register 27 (exponent register) to the entry, transfers the numeral in digit position 14 to IL, increments IH and transfers the numeral to digit position 15. The exponent units digit is now the exponent tens digit.

IH is decremented and IL exchanged with IS, bringing the new numeral back to IL. The numeral in IL is then transferred to digit position 14 and the entry stored in register 27. Register 25, containing the mantissa, is recalled to the entry and the exponent of register 27 added to the entry exponent (ADEX).

Additional numeric key depressions will result in the exponent tens digit shifting out of the entry and the most recent numeral being placed in the exponent units digit.

2.9.3 ADD OPERATION

The Add routine adds the contents of the entry register to a value stored in working memory. The computer actually executes the Add operation when the Equals key or a second algebraic key is depressed. Pressing the + key prepares the memory for entry of the augend and execution of the Add routine.

When the operator presses the + key, the computer tests the contents of column 77, register 35, byte 7. This byte contains the code of the last algebraic key. If the byte contains an algebraic code, the computer will execute that function, then prepare for the Add routine by storing the entry in column 77, register 27 (Addend Register). It also writes the Add code into column 77, register 35, byte 7, then returns to the Idle routine.

After the operator enters the number to be added (augend) and presses the = key, the computer tests register 35, byte 7 to determine the function it must execute. The Add code has been stored here, so the computer will jump to the Add routine. See Fig. 2-29.

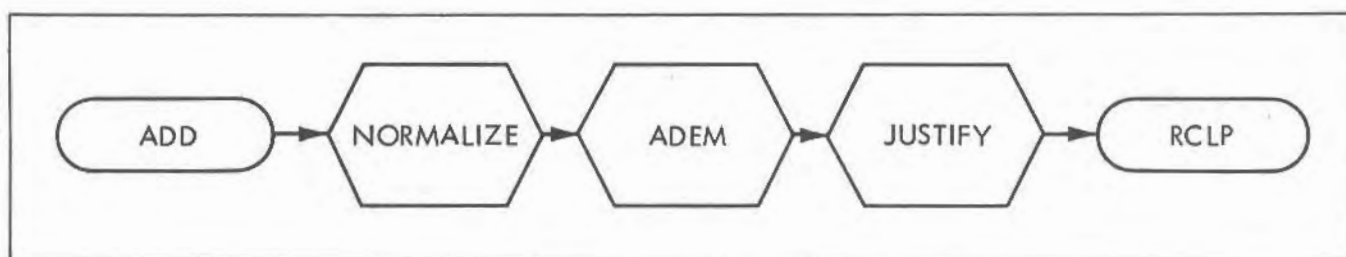


Fig. 2-29 Add Routine

To add, the computer first compares exponents of the addend and augend and normalizes the two numbers to make the exponents equal. It then transfers the addend to the Adder/Entry chip and adds the mantissas. Finally, it justifies the sum to exponential form and returns it to the Entry Register.

The computer uses the Add routine described here in the more complex functions. The routines for complex functions are, of course, considerably longer, but they too operate by executing a routine comprised of a series of stored micro-instructions.

Section III INSTALLATION AND PERFORMANCE TESTING

This section contains procedures for unpacking, installing, and testing the Compucorp Beta Computers.

3.1 INSTALLATION

The following paragraphs describe unpacking and installation of the computers.

3.1.1 UNPACKING

The computer, voltage adapter, and the 392 Cassette Drive are packed in a single carrying case, as illustrated in Fig. 3-1. To unpack the computer:

1. Open the end of the box and remove the carrying case
2. Open the carrying case
3. Remove the computer from the carrying case and place it keyboard up, on a protected surface
4. Remove the voltage adapter from the carrying case, verify that the adapter switch is set for the available line voltage, and place it beside the computer
5. Remove the 392 Cassette Drive from the carrying case and place it beside the computer.

3.1.2 SETUP

To set up the computer:

1. Connect the voltage adapter to the computer
2. Plug the voltage adapter into a power outlet of the proper voltage
3. Connect the I/O cable from the 392 Cassette Drive into the I/O Connector which is located on the lower right-hand side of the computer
4. Set the POWER switch to ON.

NOTE

The computer does not require connection of the adapter for portable use.



Fig. 3-1 Computer, Adapter and Carrying Case

3.2 PERFORMANCE TESTING

After the computer has been unpacked and set up, it is ready for test. The procedures in the remainder of this section are recommended for installation tests, as well as for problem verification and failure analysis. Par. 3.2.1 describes the recommended use of the test procedures.

3.2.1 RECOMMENDED USE OF TEST PROCEDURES

Because most complex functions use the basic add, subtract, multiply, and divide functions, the test procedures included in Tables 3-1 and 3-2 should be performed before attempting any other procedure. The procedure contained in Table 3-1 provides the SELF TEST procedure, while Table 3-2 provides the test of the basic arithmetic functions.

The test procedures contained in Tables 3-3 through 3-6 are designed to test only certain functions of the computer as indicated below:

Table 3-3 Scientist Complex Function Test

Table 3-4 Scientist Special Function Test

Table 3-5 Scientist Metric Conversion Test




Table 3-6 Programming Test

If the test procedures provided by Tables 3-1 and 3-2 are performed correctly by the computer, perform the test procedure for the function, or functions, presumed to be failing. For initial test after setup, the procedure of Tables 3-1 and 3-2 should be performed to verify proper computer operation.

The procedures provided by Tables 3-1 through 3-6 assume the computer is OFF before beginning the test procedure. Before beginning any test procedure, verify the switch positions as follows:

<u>Switch</u>	<u>Position</u>
POWER	OFF
RUN/STEP/LOAD	RUN
GRAD/DEG	DEG

Table 3-1
SELF TEST PROCEDURE

Step	Press	Verify Display	Remarks
1	Power Switch ON	0.0000	
2	  	<p>88888888888888888888</p> <p>.....</p> <p>.....</p> <p>ROM 8 . 1076</p> <p>ROM 9 . 521</p> <p>ROM A . 504</p> <p>ROM B . 351</p> <p>ROM C* . 00</p> <p>ROM D . 402</p> <p>76</p> <p>77</p>	<p>The Self Test program now executes, correct displays as indicated. The first six numbers displayed are the ROM CHECK SUMS, and the last two displayed are a RAM test. If a column of RAM memory does not check correctly, the column number is NOT displayed.</p>
3	Power Switch OFF	N/A	

*The C ROM position is not used by the Beta computer, so the number displayed in this position is disregarded.

Table 3-2
STANDARD FUNCTION TEST

Step	Press	Verify Display	Remarks
1	Power switch ON	0.0000	
2	SET D.P. EXP	0.0000000000 00	
3	SET D.P. 2	0.00	
4	SET D.P. 4	0.0000	
5	1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6	1.234567890 15	
6	CLEAR	0.0000	
7	1 ST _n 1	1.0000	
8	2 ST _n 2	2.0000	
9	3 ST _n 3	3.0000	
10	4 ST _n 4	4.0000	
11	5 ST _n 5	5.0000	
12	6 ST _n 6	6.0000	
13	7 ST _n 7	7.0000	
14	8 ST _n 8	8.0000	
15	9 ST _n 9	9.0000	
16	1 0 ST _n .	10.0000	
17	1 1 ST _n CHG SIGN	11.0000	
18	1 2 ST _n 0	12.0000	
19	RCL _n 1	1.0000	
20	RCL _n 2	2.0000	
21	RCL _n 3	3.0000	
22	RCL _n 4	4.0000	
23	RCL _n 5	5.0000	
24	RCL _n 6	6.0000	
25	RCL _n 7	7.0000	

Table 3-2
STANDARD FUNCTION TEST (Continued)

Step	Press	Verify Display	Remarks
26	RCL _n 8	8.0000	
27	RCL _n 9	9.0000	
28	RCL _n .	10.0000	
29	RCL _n CHG SIGN	11.0000	
30	RCL _n 0	12.0000	
31	EXP 4	1.0000000000 04	
32	CLEAR	0.0000	
33	8 ×	8.0000	
34	2	2.0000	
35	=	16.0000	
36	a^x 2 =	256.0000	
37	÷ 4 =	64.0000	
38	- 6 5 =	-1.0000	
39	(1 -1.0000	
40	(((4 -1.0000	
41))))	-1.0000	
42)	E-----	
43	CLEAR	-1.0000	
44	RESET	0.0000	
45	Power Switch OFF	N/A	

Table 3-3
SCIENTIST COMPLEX FUNCTION TEST

Step	Press	Verify Display	Remarks
1	Power Switch ON	0.0000	
2	8	8.0000	
3	SIN	0.1391	
4	$\frac{1}{f}$ SIN ⁻¹	8.0000	
5	COS	0.9902	
6	$\frac{1}{f}$ COS ⁻¹	7.9999	
7	TAN	0.1405	
8	$\frac{1}{f}$ TAN ⁻¹	7.9999	
9	8 $\frac{1}{f}$ TO RECT	8.0000	
10	7 =	6.9318	
11	=	0.9742	
12	8 $\frac{1}{f}$ TO POLAR	8.0000	
13	7 =	41.1859	
14	=	10.6301	
15	8 . 5 8 $\frac{D/M/S}{\square}$	8 34 48.0000	
16	$\frac{1}{f}$ X \leftrightarrow DEC	8.5800	
17	$\frac{1}{f}$ X \leftrightarrow DEC	8 34 48.0000	
18	$\frac{1}{f}$ X \leftrightarrow DEC	8.5800	
19	GRAD DEG	N/A	
20	8	8.0000	
21	TO RECT	8.0000	
22	7 =	6.9448	
23	=	0.8773	
24	8 $\frac{1}{f}$ TO POLAR	8.0000	
25	7 =	45.7621	
26	=	10.6301	
27	8 . 5 8 $\frac{D/M/S}{\square}$	8 34 48.0000	
28	$\frac{1}{f}$ X \leftrightarrow DEC	8.5800	

Table 3-3
SCIENTIST COMPLEX FUNCTION TEST (Continued)

Step	Press	Verify Display	Remarks
29		N/A	
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48	Power Switch OFF	N/A	

Table 3-4
SCIENTIST SPECIAL FUNCTION TEST

Step	Press	Verify Display	Remarks
1	Power Switch ON	0.0000	
2	f 1 ST_n 1	2.7182	e in entry
3	CHG SIGN	-2.7182	
4	f 2	2.7182	Absolute value
5	f 7 ST_n 2 ST_n 3	3.1415	π in entry
6	f 0	N/A	Clear 1, 2, 3
7	RCL _n 1	0.0000	
8	RCL _n 2	0.0000	
9	RCL _n 3	0.0000	
10	f 7	3.1415	
11	f 8	3.1416	Round to DP
12	2 Σ_{max}	2.0000	
13	3 Σ_{max}	3.0000	
14	f 3	2.5000	Mean
15	f 4	0.7071	SD
16	1 0 5 .		
	5 0 1	105.501	
17	f 5	0.5010	Fraction
18	1 0 5 .		
	5 0 1	105.501	
19	f 6	105.0000	Integer
20	f 9	105.	Display Identifier
21	4 ST_n 4	4.0000	
22	5 ST_n 5	5.0000	
23	6 ST_n 6	6.0000	
24	7 ST_n 7	7.0000	
25	8 ST_n 8	8.0000	
26	9 ST_n 9	9.0000	

Table 3-4
SCIENTIST SPECIAL FUNCTION TEST (Continued)

Step	Press	Verify Display	Remarks
27	1 0 ST_n .	10.0000	Clear entry and data memory
28	1 1 ST_n CHG SIGN	11.0000	
29	1 2 ST_n 0	12.0000	
30	CLEAR	0.0000	
31	RCL_n 1	0.0000	
32	RCL_n 2	0.0000	
33	RCL_n 3	0.0000	
34	RCL_n 4	0.0000	
35	RCL_n 5	0.0000	
36	RCL_n 6	0.0000	
37	RCL_n 7	0.0000	
38	RCL_n 8	0.0000	
39	RCL_n 9	0.0000	
40	RCL_n .	0.0000	
41	RCL_n CHG SIGN	0.0000	
42	RCL_n 0	0.0000	
43	Power Switch OFF	N/A	

Table 3-5
SCIENTIST METRIC CONVERSION TEST

Step	Press	Verify Display	Remarks
1	Power Switch ON	0.0000	
2	8 METRIC 0	-13.3333	°F to °C
3	METRIC 0	8.0000	°C to °F
4	METRIC 1	20.3200	in. to cent.
5	METRIC 1	8.0000	cent. to in.
6	METRIC 2	2.4384	feet to meters
7	METRIC 2	8.0000	meters to feet
8	METRIC 3	12.8747	mi. to km.
9	METRIC 3	8.0000	km. to mi.
10	METRIC 4	131.0965	in ³ to cm ³
11	METRIC 4	8.0000	cm ³ to in ³
12	METRIC 5	30.2832	US gals. to liters
13	METRIC 5	8.0000	liters to US gals.
14	METRIC 6	36.3687	UK gals. to liters
15	METRIC 6	8.0000	liters to UK gals.
16	METRIC 7	3.6287	lbs. to kg.
17	METRIC 7	8.0000	kgrams to lbs.
18	METRIC 8	226.7961	oz. to grams
19	METRIC 8	8.0000	grams to oz.
20	METRIC 9	0.1281	lbs/ft ³ to gm/cm ³
21	METRIC 9	8.0000	gm/cm ³ to kg/cm ³
22	METRIC .	0.5624	lbs/in ² to kg/cm ²
23	METRIC .	8.0000	kg/cm ² to lbs/in ²
24	METRIC CHG SIGN	0.1396	deg. to radians
25	METRIC CHG SIGN	8.0000	radians to deg.
26	METRIC CHG SIGN	8.0000	
27	METRIC CHG SIGN	0.1256	grads to radians
28	METRIC CHG SIGN	8.0000	radians to grads
29	Power Switch OFF		

Table 3-6
PROGRAMMING TEST






















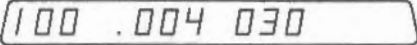

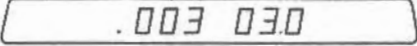

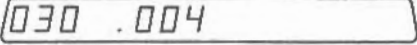

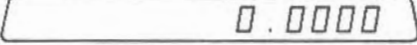
Step	Press	Verify Display	Remarks
1	Power Switch ON	0.0000	
2		.001	
3		033 .002	
4		001 .005	
5		002 .008	
6		003 .011	
7		004 .014	
8		114 .017	
9		114 .020	
10		114 .023	
11		114 .026	
12		0.0000	
13		- - - - -	
		1.0000	
		- - - - -	
		2.0000	
		- - - - -	
		3.0000	
		- - - - -	
		4.0000	
		- - - - -	
		4.0000	
14		4 0000	
15		033 .002 001 300	
		1.0000	
16		001 .003 300 001	
		1.0000	

Table 3-6
PROGRAMMING TEST (Continued)

Step	Press	Verify Display	Remarks
17		001 .005 002 300 2.0000	
18		002 .006 300 002 2.0000	
19		002 .008 003 300 3.0000	
20		003 .009 300 003 3.0000	
21	Power Switch OFF		Wait 3 seconds
22	POWER SWITCH ON	0.0000	
23		.001	
24		.002	
25		.001	
26		350 .002	
27		354 .002	
28		355 .002	
29		357 .002	
30		100 .002	
31		200 .002	
32		202 .002	
33		360 .003	
34		364 .003	
35		365 .003	
36		367 .003	
37		203 .003	
38		030 .004	
39		203 .003 030	
40		202 .002 203 030	

Table 3-6
PROGRAMMING TEST (Continued)

Step	Press	Verify Display	Remarks
41			
42			
43			
44			
45			
46			
47	POWER SWITCH OFF		

Section IV DISASSEMBLY

Initial problem isolation is most often accomplished by assembly substitution. Section IV details the recommended procedure for removal and replacement of the computer assemblies.

4.1 COVER REMOVAL AND REPLACEMENT

To remove the cover:

1. Turn the POWER switch to OFF and disconnect the voltage adapter
2. Open the battery door; grasp one side of the door while holding the computer in place with the other hand and tug the door. The door will snap out, allowing easy access to the screws in the battery compartment
3. Place the computer upside down on a protective surface
4. Remove the two rubber feet
5. Using a Phillips-head screwdriver, remove the six screws shown in Fig. 4-1

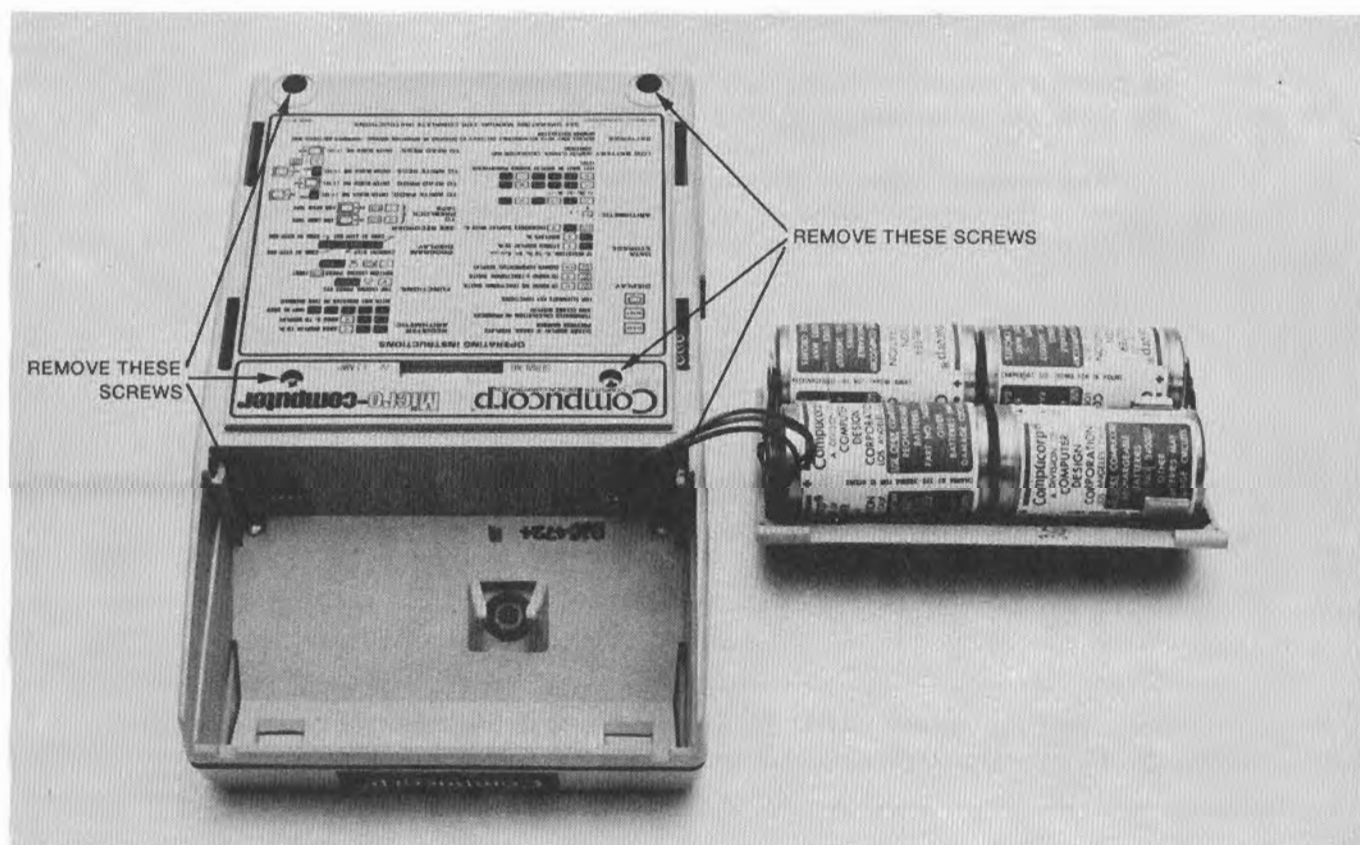


Fig. 4-1 Cover Removal and Replacement

6. Place the computer right side up and carefully lift the top cover. Remove the slide switch buttons
7. Carefully lift the chassis assembly out of the bottom cover
8. Disconnect the power cable from the Converter Board
9. Remove the two circuit board spacers.

To reinstall the cover:

1. Verify that all boards are properly seated
2. Verify that the power cable from the battery compartment goes to the chassis compartment through the right-hand opening (as viewed from the front)
3. Replace the circuit board spacers
4. Place the chassis assembly in the bottom cover, ensuring that the power cable does not shift out of position, and connect the power cable
5. Turn the computer upside down and install the two short Phillips-head screws in the holes on each side of the serial number
6. Turn the computer right-side-up and check the slide switches for proper settings as listed in Table 4-1
7. Mate the top cover with the bottom cover, ensuring that none of the wires are pinched and the I/O connector is not damaged
8. Turn the computer upside-down and install the two long Phillips-head screws in the holes exposed by removal of the rubber feet. Do not completely tighten the screws

Table 4-1
SLIDE SWITCH SETTINGS FOR REASSEMBLY

Model	Switch Settings				
	SS1	SS2	SS3	SS4	SS5
326	X	X	Down	Down	X

An "X" indicates that the switch setting for reassembly is unimportant because the switch is accessible to the operator or has no effect on that model.

9. Install the two Phillips-head screws in the battery compartment. Tighten these screws, and those installed in steps 5 and 8
10. Turn the computer right-side-up, turn the POWER switch to ON, and verify proper operation of the computer
11. When correct operation has been verified, reinstall the battery door by snapping it into place. Reinstall the rubber feet. Reconnect the voltage adapter if desired.

4.2 DISPLAY SHROUD REMOVAL AND REPLACEMENT

To remove the display shroud:

1. Remove the top cover as indicated by Par. 4.1
2. Turn the top cover upside-down, and push the display shroud through the opening in the top cover
3. Remove the display shroud.

To reinstall the display shroud:

1. Turn the top cover upside down and install the display shroud
2. Reassemble the computer as indicated by Par. 4.1.

4.3 KEYBOARD REMOVAL AND REPLACEMENT

To remove the keyboard:

1. Remove the cover (Par. 4.1)
2. Remove the two grip-rings holding the keyboard in place
3. Carefully slide the keyboard cable clamp off the keyboard connector.

To reinstall the keyboard:

1. Reconnect the keyboard cable on the keyboard. Carefully inspect the cable, cable clamp, and the pins on the board to insure proper alignment
2. Place the keyboard atop the chassis, ensuring that the alignment pins pass through the holes in the keyboard assembly
3. Reinstall the grip-rings on the alignment pins
4. Replace the cover (Par. 4.1).

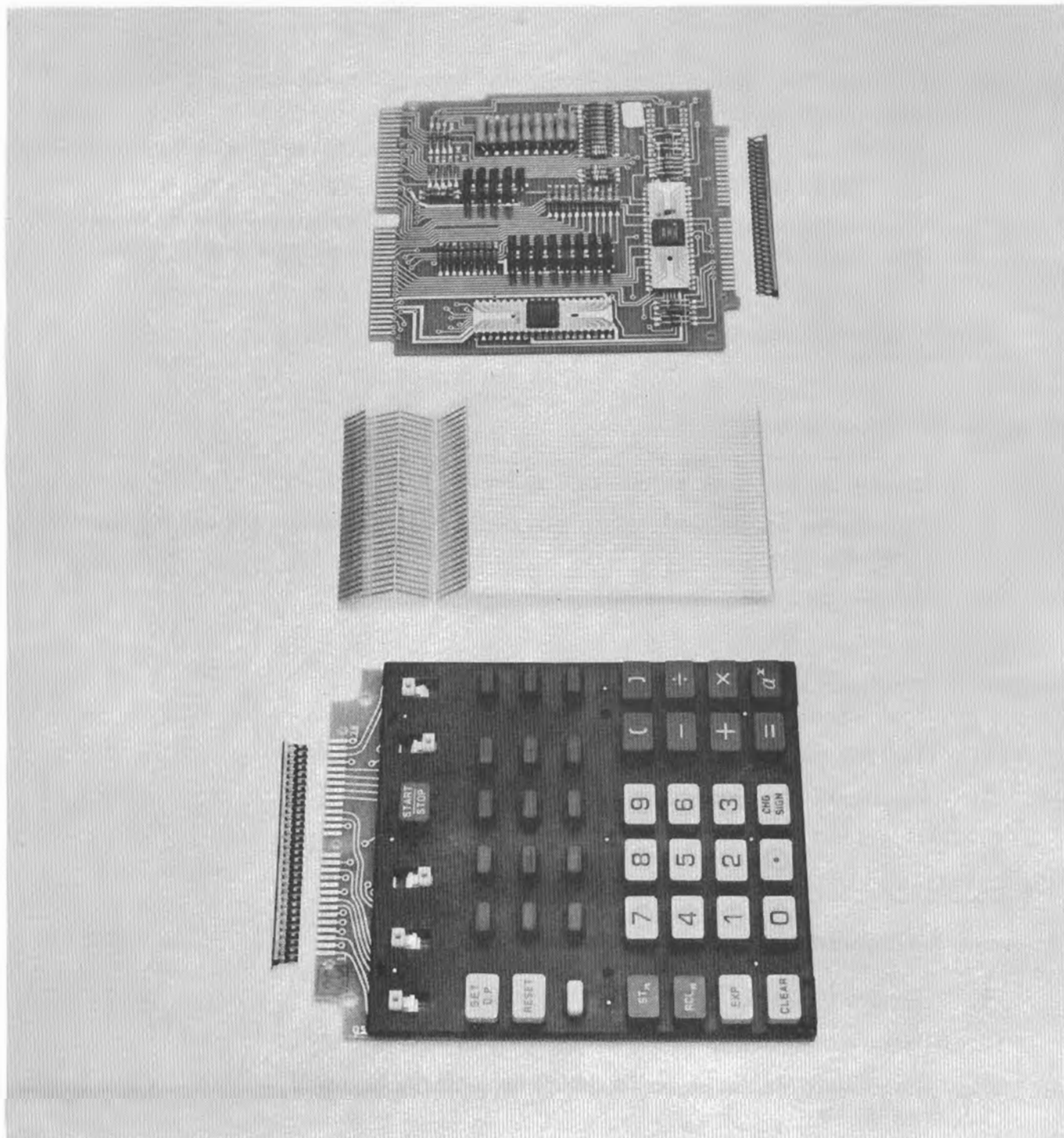


Fig. 4-2 Keyboard Removal and Replacement

4.4 KEYBOARD DISASSEMBLY AND REASSEMBLY

To disassemble the keyboard:

1. Remove the keyboard as described in Par. 4.3
2. Place the keyboard upside down on a protective surface

3. Remove the eight screws holding the circuit board to the actuator plate
4. Lift the printed circuit board. The metal dome and slide switch contacts may be lifted from their recesses
5. To remove a keyswitch actuator, pull the keybutton off the actuator stem and lift out the actuator.

To reassemble the keyboard:

1. Place the actuator plate upside down on a protective surface
2. Place any actuators previously removed in the plate recesses; place the metal domes atop the actuators concave side up. Place the slide switch contacts in their recesses
3. Align the circuit board on the plate and reinstall the eight screws. Test all switches for proper feel. Reinstall any keybuttons previously removed
4. Reinstall the keyboard per Par. 4.3.

4.5 DISPLAY REMOVAL AND REPLACEMENT

To remove the display:

1. Remove the cover per Par. 4.1
2. Grasp the display firmly and slowly pull the display off the connector. The display interconnect may be unplugged from the terminal block if necessary. See Fig. 4-3.

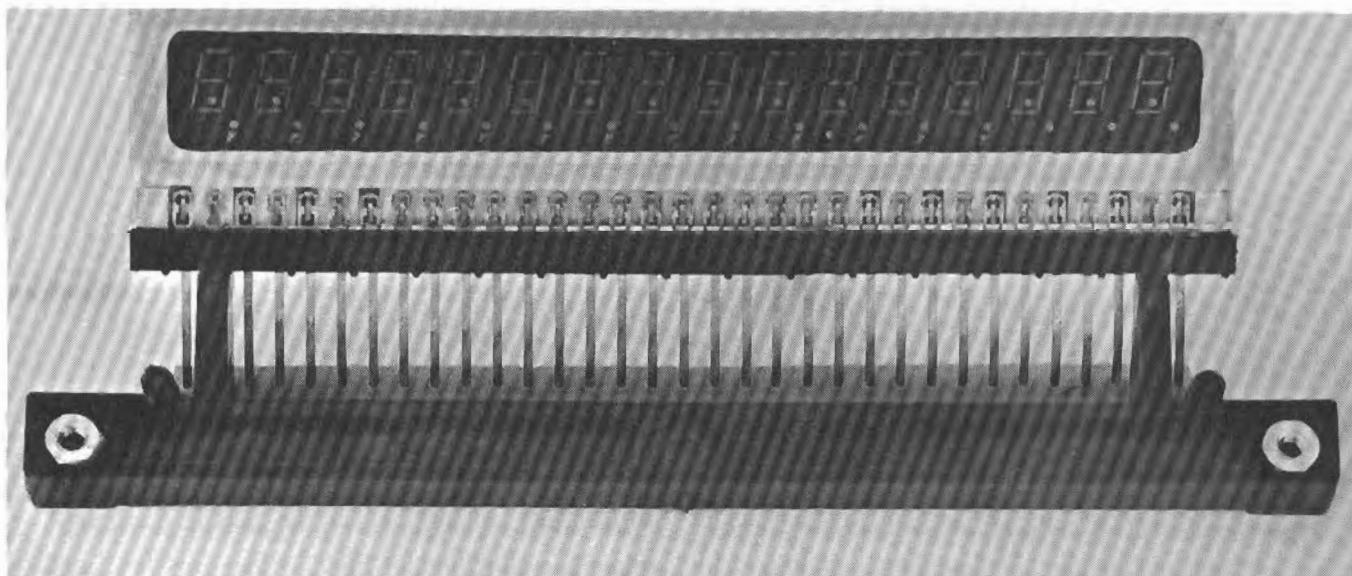


Fig. 4-3 Display Removal and Replacement

To reinstall the display:

1. Seat the display assembly firmly on the interconnect assembly and check for the proper alignment. Take extreme care that the connector fingers are not damaged
2. Replace the cover per Par. 4.1.

4.6 PRINTED CIRCUIT BOARD REMOVAL AND REPLACEMENT

To remove a printed circuit board:

1. Remove the cover as described in Par. 4.1
2. Pull the circuit board out of the terminal block. If necessary, a small flat-blade screwdriver may be used to pry the board, but exercise caution to avoid damage to the components and printed circuits. When removing the Control Assembly, take care to avoid damage to the I/O connector.

To reinstall a printed circuit board:

1. Align the board with the opening in the terminal block and push it into place. Ensure that the board is all the way in and that it is properly aligned
2. Reinstall the cover as described in Par. 4.1.

4.7 BATTERY CLIP REMOVAL AND REPLACEMENT

To replace a defective battery clip, perform the following procedure:

1. Turn off the POWER switch and remove the batteries
2. Remove the Phillips-head screw securing the defective clip to the battery door
3. Unsolder the wire from the clip
4. Solder the new clip to the wire
5. Install the screw removed in step 2
6. Reinstall the batteries and turn on the computer. Verify proper operation of the machine.

4.8 POWER SWITCH REMOVAL AND REPLACEMENT

To replace a defective power switch, perform the following procedure:

1. Turn off the POWER switch and remove the batteries
2. Unsolder the two wires from the switch
3. Remove the Phillips-head screws in the center of the battery door which secure the battery clips to the door
4. Snap out the battery door cover
5. Replace the defective switch and reinstall the battery door cover and screws
6. Solder the wires on to the new switch
7. Reinstall the batteries. Turn on the computer and verify proper operation.

4.9 VOLTAGE ADAPTER CONNECTOR REMOVAL AND REPLACEMENT

To replace a defective voltage adapter connector, perform the following procedure:

1. Turn off the POWER switch and remove the batteries
2. Remove the Phillips-head screws in the center of the battery door and secure the battery clips to the door
3. Snap out the battery door cover
4. Remove the two screws securing the connector to the battery door
5. Unsolder and tag the wires
6. Replace the defective connector
7. Replace the screws removed in step 4; resolder the wires
8. Reinstall the battery door cover and reinstall the screws removed in step 2
9. Reinstall the batteries. Turn on the computer and verify proper operation.

4.10 VOLTAGE ADAPTER DISASSEMBLY AND REASSEMBLY

To disassemble the voltage adapter:

1. Remove the four Phillips-head screws from the bottom and lift off the top cover
2. Remove the two Phillips-head screws holding the circuit board and the two screws which hold the voltage adapter switch in place (Fig. 4-4)
3. Remove the circuit board, the transformer, and the adapter switch.

To reassemble the voltage adapter:

1. Place the printed circuit board, the transformer, and adapter switch in position
2. Reinstall the Phillips-head screws and reposition the strain reliefs in the openings of the bottom cover
3. Place the top cover in position and install the Phillips-head screws through the bottom cover.

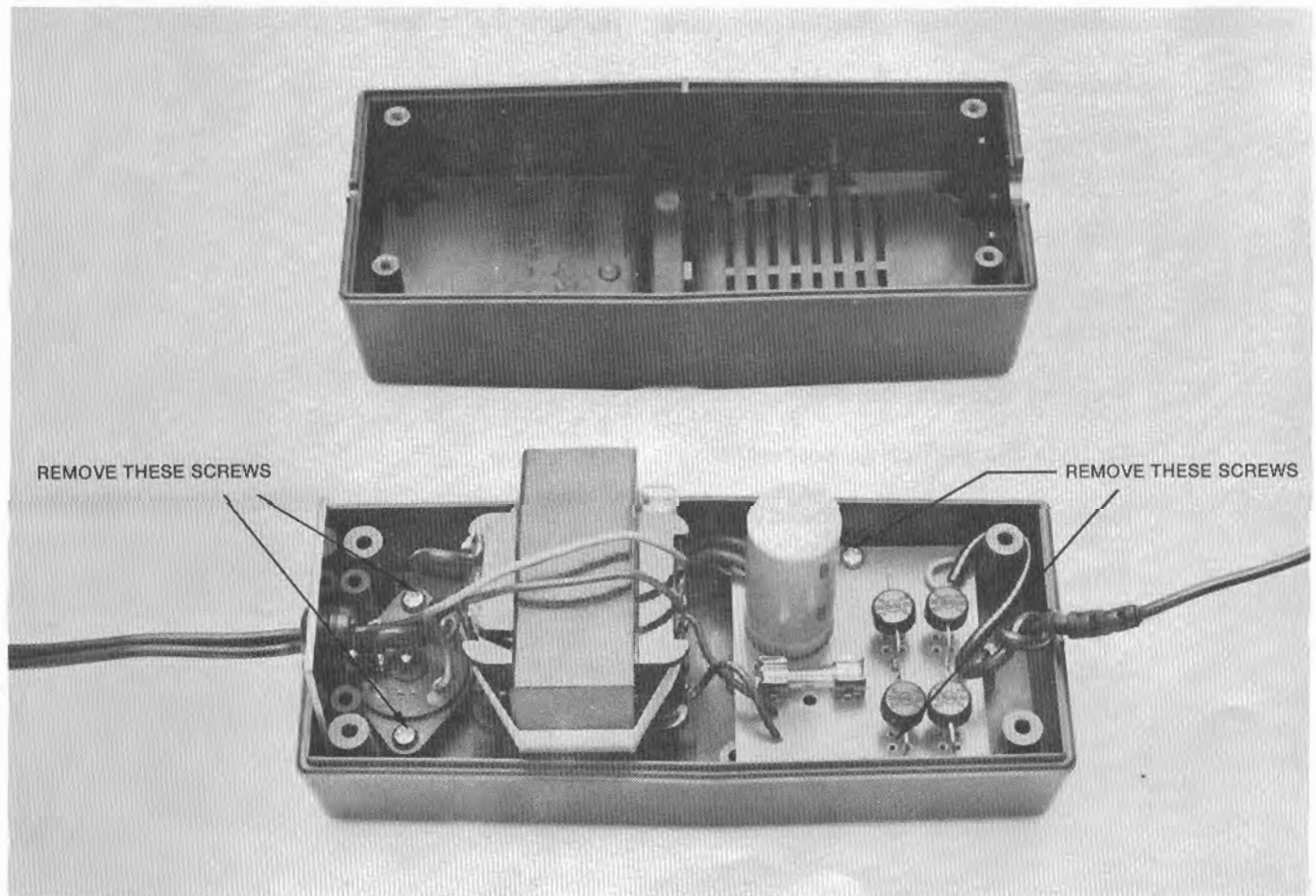


Fig. 4-4 Voltage Adapter Disassembly

Section V FAILURE ANALYSIS AND REPAIR

Section V contains general guidelines for localizing a problem to a subassembly. It also includes some general considerations that the technician should observe when making repairs.

5.1 FAILURE ANALYSIS

Trouble isolation is accomplished by obtaining information from the answers to calculations and then logically applying this information to locate a defective assembly or component. When a computer malfunction is first suspected, disconnect all peripheral devices before attempting to verify the failure; then attempt to isolate the malfunction quickly by visual and operational checks. Ensure that a problem is actually the result of a malfunction and not improper switch settings or attempts to perform illegal operations.

A sequential test usually provides more reliable information for analysis than indications taken from regular operation. The checkout procedures in Section III are recommended, since they test the simplest functions before proceeding to the more difficult operations. All subroutines for the more complex operations access subroutines used in simpler calculations; therefore, failure of a simple function would probably affect the results of a complex calculation.

Most failures result from defective semiconductors or integrated circuit chips. Because of the interdependence of the circuits, it is often impossible, without special test equipment, to provide a procedure that will isolate the problem to a particular assembly or component. Troubleshooting is greatly simplified when a suspect assembly can be replaced with one known to be operating correctly.

Table 5-1 lists possible causes of the more common problems. This table has been compiled from failure histories and is not intended to include all possible failures and their causes.

5.1.1 VOLTAGE ADAPTER

If the batteries will not recharge or if the computer operates from batteries but not from the voltage adapter, the adapter should be replaced.

Table 5-1
POSSIBLE FAILURE CAUSES

FAILURE INDICATION	Voltage Adapter	Power Distribution Assembly	Converter	Display Drive	Data File	Control	Display and Interconnect	Keyboard	Keyboard Cable
Incorrect Entry			X			X			
Incorrect Display			X			X	X		
Incorrect Voltage	X	X							
Intermittent					X				
Heat Sensitive					X	X			
No Reset			X	X			X	X	
Missing Segments			X				X		
Blinking Display	X	X	X						
No Display	X	X	X						X
Missing Digit			X				X		
No Power	X	X							
Power-On Routine Failure					X	X			
Inoperative with Batteries	X								
Single Key Failure							X	X	
Batteries do not Recharge	X	X	X						
Overheats	X	X	X						
No Power with Adapter	X	X							
Lockup			X	X	X		X	X	
Incorrect Program				X	X				
Incorrect Math Functions		X		X	X				
Incorrect Store/Recall				X	X				
Peripheral		X	X	X	X				

5.1.2 CONVERTER

A Converter malfunction can cause a wide range of failure indications, from a completely inoperative machine to intermittently incorrect answers. The exact indication will depend on the nature of the failure and the tolerance of the logic circuits to voltage variations.

If the computer will not operate at all, exchange the batteries and voltage adapter before disassembling the computer to replace the Converter.

5.1.3 DISPLAY DRIVE ASSEMBLY

Some Display Drive failures will appear as incorrect entries or incorrect displays. The Display Drive assembly would normally be the first assembly substituted when these symptoms appear.

The Display Drive assembly also contains the Read circuits for peripheral data. If a peripheral failure is apparent, the Display Drive assembly should be the first assembly substituted.

5.1.4 CONTROL ASSEMBLY

A control malfunction may cause anyone of the following symptoms: incorrect entry, incorrect display, lockup, program failure, incorrect answers, and incorrect storage and recall.

The interrupt control circuits and the data output circuits for the peripheral devices are also on the Control assembly. If the 392 Cassette Drive pre-blocks a blank tape, but does not read or write on the same tape, the Control assembly should be the first assembly substituted.

5.1.5 DATA FILE ASSEMBLY

Many Data File failure indications resemble those for Control. However, timing for peripheral input/output operations is generated by microprograms within the computer memory. If a peripheral timing problem is apparent, the Data File assembly would normally be the first assembly substituted.

5.2 REPAIR

The following paragraphs contain repair information of a general nature. All personnel repairing any computers should be familiar with the safety and service precautions as well as the other information applicable to their particular tasks.

5.2.1 SAFETY PRECAUTIONS

The Converter generates two potentially lethal voltages; the AC line voltage also may inflict a fatal shock. These voltages are present at several points with the computer turned on and the cover removed. To avoid shock, observe the following precautions:

1. Provide ample illumination
2. Avoid wearing wrist watches, rings or other metal articles which may accidentally contact a high-voltage point
3. Isolate yourself from ground by standing on an insulating mat
4. Use only one hand when making tests or adjustments on energized equipment
5. Turn off the machine before removing or installing any circuit boards or other components
6. After turning off the computer, discharge the high-voltage filter capacitors on the Converter Board (C7 and C8) before touching the board. To prevent damage to the Converter, discharge the capacitors through a 1K ohm resistor, not with a jumper wire or screwdriver.

5.2.2 SERVICE PRECAUTIONS

MOS/LSI chips are highly susceptible to damage by static discharges and reversed voltages. Other semiconductors, as well as the printed circuits, are easily damaged by improper handling and overheating. To prevent avoidable damage, observe the following precautions:

1. Avoid unnecessary handling of printed circuit boards
2. Before touching a board, discharge your body to the grounded metal bench or chassis
3. When it is necessary to handle a board, hold it by the edges without touching the circuits or components

4. When a board out of a machine is not being worked on, keep it in an antistatic bag.
5. All service equipment connected to the AC line must be grounded. Use only 3-wire grounded soldering irons. Do not use soldering guns
6. When making an ohmmeter check between two points going to an MOS chip, connect the test leads so the voltage applied to the chip is the same polarity as in normal operation
7. When working on an energized machine, use test probes and metal tools with extreme caution to avoid accidental shorts
8. Apply the soldering iron only long enough to form a proper joint
9. Remove a board from the machine before soldering
10. Never service a machine on a metal-top bench
11. Turn the computer OFF before removing or installing an assembly or disconnecting a connector. Discharge the high-voltage capacitors on the Converter board through a 1K-ohm resistor before removing the board
12. Install components as close to the board as possible and, on the far side of the board, clip all leads as close as possible to avoid shorts.

5.2.3 CIRCUIT BOARD CHECKOUT

Some general instructions for testing and troubleshooting the printed circuit boards are described below; other methods may be developed according to individual experience and preference. Sections VI through XI contain information applicable to checkout and repair of the various printed circuit boards. Because of the interdependence of the MOS/LSI logic, all procedures in this manual assume that the computer is fully operational except for the board under test.

5.2.3.1 Special Tools and Test Equipment

In addition to the standard tools used in servicing electronics equipment, the following equipment is required for testing and troubleshooting the circuit boards:

1. A working Beta computer compatible with the assembly under test
2. Recommended tools and test equipment listed in Table 5-2.

Table 5-2
RECOMMENDED SPECIAL TOOLS AND TEST EQUIPMENT

Item	Type Required
Desoldering Tool	Solder Pullit
Soldering Iron	Weller 24V, 60W with grounded tip and transformer
Vohmmeter	Simpson 260, or equivalent
Oscilloscope	Tektronix 432 with P6006 probe*
Wire Stripper	Miller 106
Velostat Sheet	1705-1
Substitution Adapter	40-pin ACL 0142646
Substitution Adapter	40-pin TCL 0142638
Substitution Adapter	28-pin ROM 0142653
Substitution Adapter	16-pin RAM 0142661
Extender Boards	0144626, 0144634
Snap Ring Pliers	TRUARC S152

*If a P6006 probe is not available, a Tektronix P6008 probe may be used.

5.2.3.2 Use of Substitution Adapters

To use the adapters in substituting the ACL, TCL and ROM chips:

1. With the test computer OFF, install the defective circuit board in the computer on an extender board
2. Set the clamping lever of the adapter at a right angle to the adapter socket
3. Insert the substitute chip in the adapter socket with pin 1 nearest the clamping lever. (See Fig. 5-1 for pin identification.)
4. Set the clamping lever in line with the adapter socket
5. Spread the jaws of the adapter and clamp it onto the suspect chip so the pins of the substitute are directly over the corresponding pins of the original chip
6. Carefully inspect the connection of the adapter to the original chip to ensure they are properly mounted. This is especially necessary when the chip is mounted close to the board and should be standard practice when using the adapter

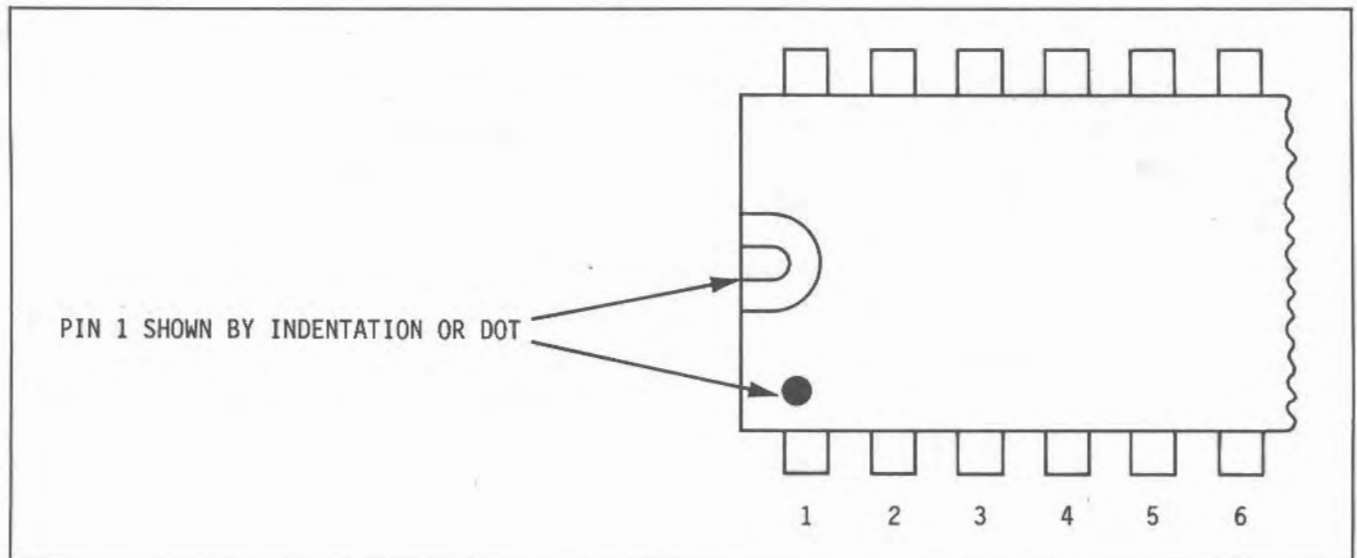


Fig. 5-1 Pin Identification

7. Turn the computer ON
8. Perform the tests required to check the malfunction. If a malfunction appears which differs from the one present when the original chip is active, reinspect the mating of the adapter with the original chip
9. When the tests are complete, turn the computer OFF and remove the adapter, then remove the chip from the adapter by setting the clamping lever at a right angle to the socket and lifting the chip out
10. Repeat steps 3 through 9 for each chip on the board until the problem disappears or all chips have been tested.

CAUTION

Always ensure the computer is OFF before mounting or removing the adapter. Failure to observe this precaution may destroy the original, substitute, or both chips.

Substitution of the 1K RAM chips requires a slightly different procedure. To use the RAM substitution adapter:

1. With the test computer OFF, install the defective circuit board in the computer on the extender board
2. Insert the substitute RAM in the adapter socket so that pin 13 goes into the connector having the Q-ball probe attached
3. Spread the jaws of the adapter and clamp it onto the suspect chip so the pins of the substitute chip are directly over the corresponding pins of the original chip
4. Connect the Q-ball to pin 15 of shift register Z9 or to the end of either R19, R20, R21 or R22 which goes to Z10-15

5. Carefully inspect the connection of the adapter to the original chip to ensure they are properly mated. This is especially necessary when the chip is mounted close to the board and should be standard practice when using the adapter
6. Turn the computer ON
7. Perform the tests required to check the malfunction. If a malfunction appears which differs from the one present when the original chip is used, reinspect the mating of the adapter with the original chip
8. When the tests are complete, turn the computer OFF and remove the adapter
9. Repeat steps 3 through 8 until all suspect RAMs have been tested.

CAUTION

Always ensure the computer is OFF before mounting or removing the adapter. Failure to observe this precaution may destroy the original, substitute, or both chips.

5.2.4 PARTS SUBSTITUTION

In some instances, an exact replacement for an assembly or component will not be available, but may be replaced by an equivalent part. The purpose of the following paragraphs is to clarify acceptable substitutions.

5.2.4.1 Voltage Adapter Usage

The voltage adapter approved for use with the Beta Computer is the 117/220/240 VAC version, Compucorp P/N 3490059.

5.2.4.2 Chip Interchangeability

Table 5-3 lists the chip substitutions approved at the time this manual was published. For the most recent list of substitutes refer to the latest revision of the "Approved Substitution List," document number 0000737 and the "Substitution List Addendum," document number 0020271.

Substitution information for the ROM and RAM chips is included in Section XI (Data File Checkout and Repair). The ACL or TCL combinational logic chips used in the CompuCorp 400 Maxi Series are NOT acceptable in the computer because those chips have not passed the low voltage tests required for use in the computer.

5.2.4.3 Discrete Component Substitution

This manual does not list substitutes for discrete components because of the large number of possibilities. The officially approved substitutes are included in the lists described in Par. 5.2.4.2.

If emergency conditions require the substitution of a component not listed, ensure that the physical size of the substitute part is compatible with the high component density and tight circuit board spacing of the computer; otherwise, short circuits could seriously damage the machine.

Table 5-3
INTEGRATED CIRCUIT SUBSTITUTION LIST

Original Part		Acceptable Substitute	
Part Number	Description	Part Number	Description
0440099	Fairchild 93L00N	0440099	Advanced Micro Device UGM 93L0059
		0440206	T.I. SN74LS195N
0440149	T.I. SN74L75N	0440149	T.I. SN64L75N
		0440248	T.I. SN54L75N
		0440248	National DM54L75N
0440164	T.I. SN74L93N	0440255	T.I. SN54L93N
0450114	T.I. SN74L00N	0450296	T.I. SN74LS00N
		0450247	National DM74L00N
0450148	T.I. SN74L04N	0450213	National DM74L04N
		0450320	T.I. SN74LS04N

Section VI

VOLTAGE ADAPTER CHECKOUT AND REPAIR

Section VI contains information for testing and repairing the voltage adapter used with the Beta computer.

6.1 AC ADAPTER CHECKOUT

The fastest means of testing an AC adapter is to plug it into an AC outlet supplying the proper voltage and connect and output plug to a computer from which the batteries have been removed. If the computer operates correctly and the display does not flash, the adapter may normally be considered satisfactory.

When a more detailed test is desirable, the adapter may be tested against the specifications listed below. Since the adapter does not regulate the output, some variation is normal, but there should be no extreme deviation from these specifications:

Output: 5.5 volts minimum at 1.5 amperes
6.5 volts ± 0.5 volts at 1.2 amperes
9-11 volts at 0.35 amperes
12-14 volts at no load

Ripple: 2.2 volt peak-to-peak at 1.4 amperes

All measurements are taken at the output plug.

6.2 AC ADAPTER FAILURE ANALYSIS

Figure 6-1 is a flow-chart of suggested troubleshooting procedures for the 117/220/240 VAC adapter. The schematic diagram, Fig. 6-2, and the assembly drawing, Fig. 6-3, are provided for reference. It is necessary to partially disassemble the adapter as described in Par. 4.10.

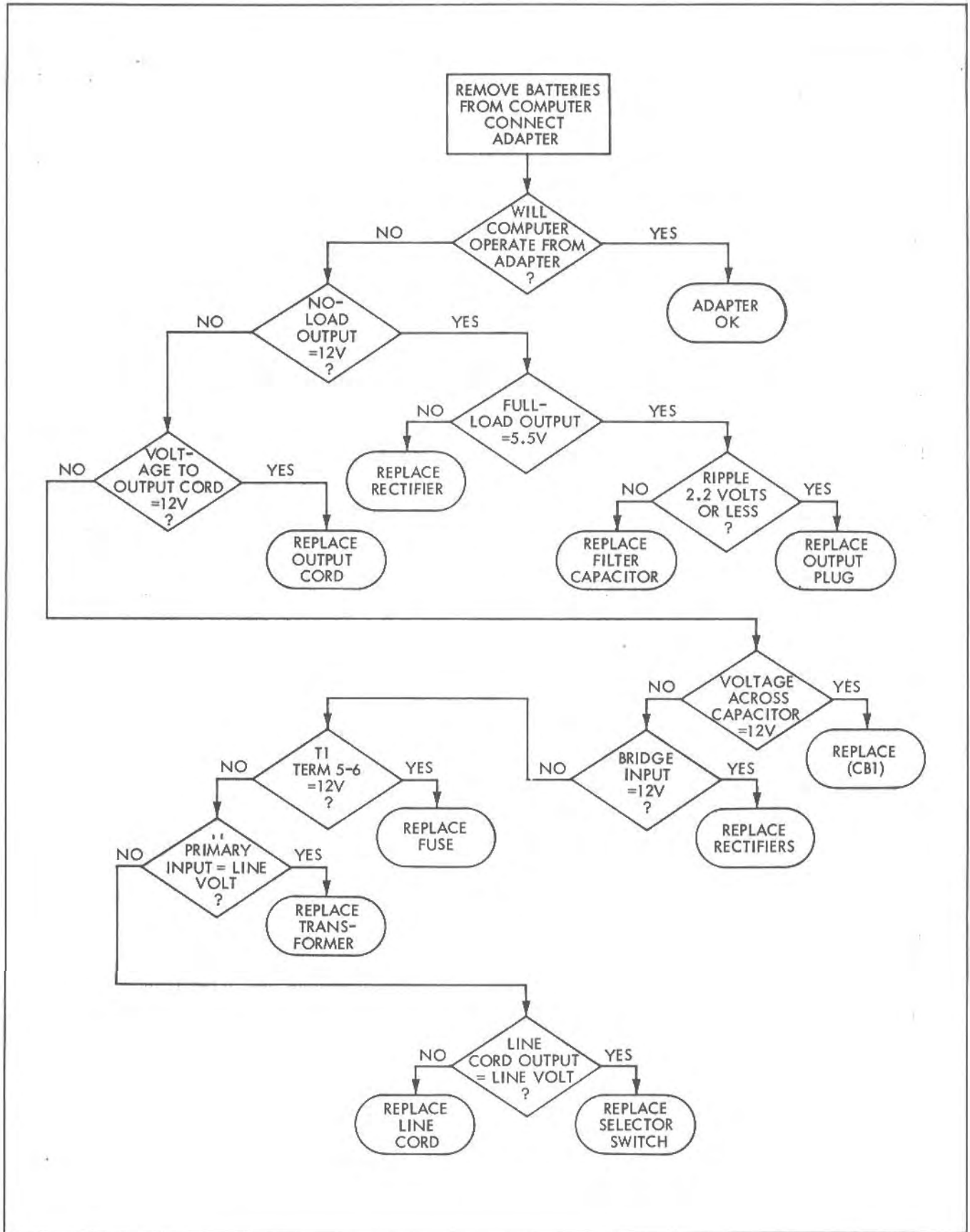


Fig. 6-1 AC Adapter Troubleshooting Flow Chart

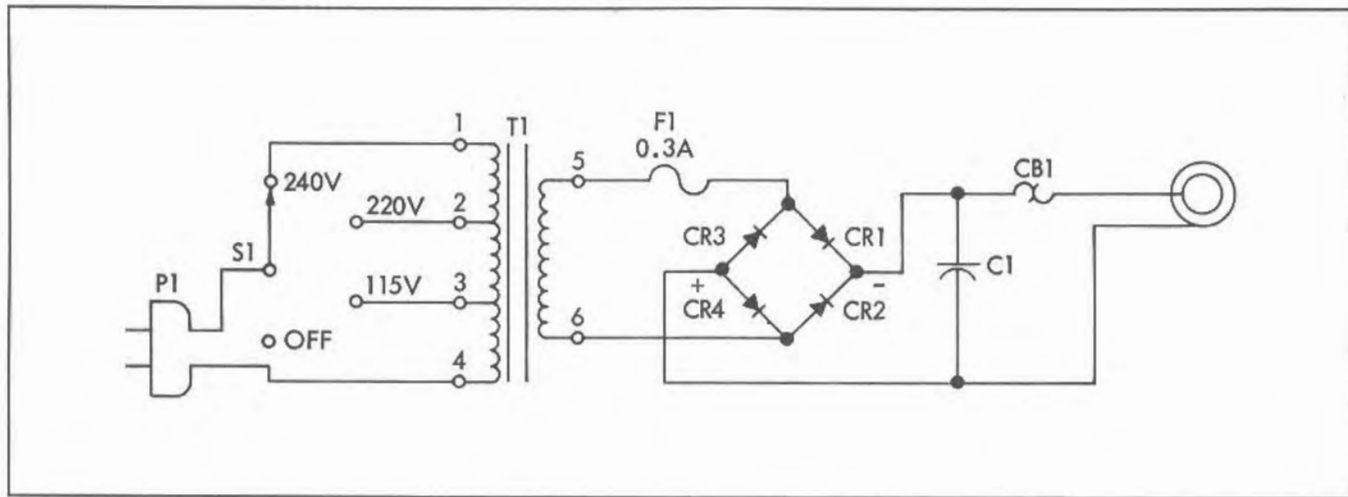
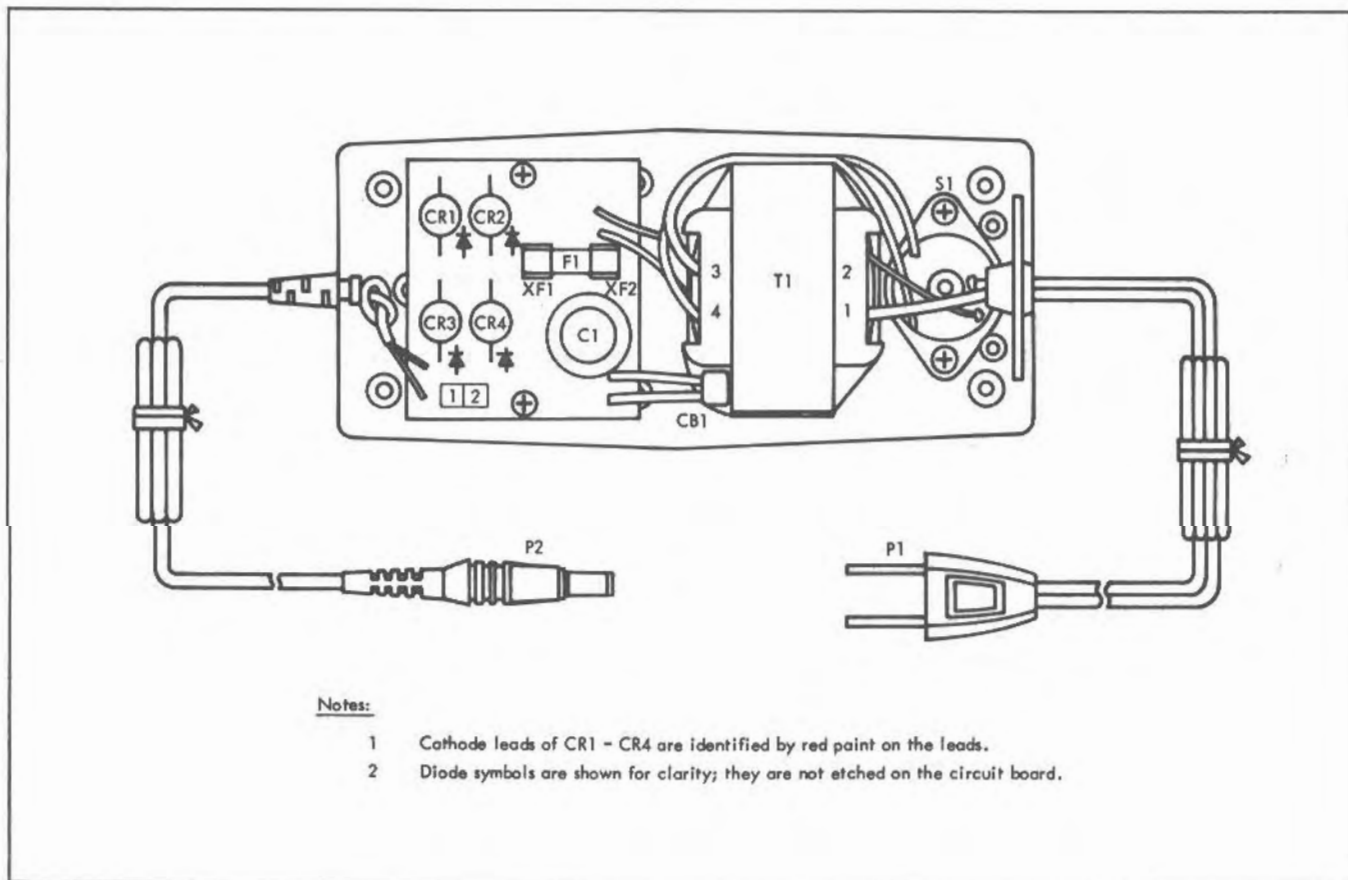


Fig. 6-2 AC Adapter Schematic Diagram



Notes:

- 1 Cathode leads of CR1 - CR4 are identified by red paint on the leads.
- 2 Diode symbols are shown for clarity; they are not etched on the circuit board.

Fig. 6-3 AC Adapter Assembly

Section VII
POWER SYSTEM CHECKOUT AND REPAIR

Section VII provides guidelines for troubleshooting the power system. When the computer exhibits a power problem, first localize the defect to one of the power assemblies: batteries, power distribution assembly or Converter board. It is assumed that the voltage adapter has been eliminated as a possible cause.

7.1 BATTERIES

If the computer operates from the voltage adapter, but not from the batteries, first ensure the batteries are installed with the correct polarity. Next, replace the batteries with fully-charged cells in good condition. If good batteries do not correct the problem, check the power distribution assembly.

Batteries which have been subject to excessive charging current may be defective. Batteries which will not output 1.2 volts at 1.1 amperes after recharging should be replaced. Any battery which does not produce 1.2 volts open-circuit or is corroded should be discarded with no attempt at recharging.

Only rechargeable, pressure-vented batteries should be installed in the computer. Other batteries may result in damage to the equipment. Engineering-approved batteries (at the date of publication) are listed in Table 7-1.

Table 7-1
APPROVED BATTERIES

Vendor	Vendor Part Number	Compucorp Part Number
General Electric	41B004AD07G2	3400017
Gould	400469-405	3400017
Varta	RS-4	3400017
Marathon	S103	3400025
Sanyo	N3500D	3400025
Saft	R360	3400025

The Marathon battery is rated for only three ampere-hours as compared to the 3.5-4 ampere-hour rating of the other batteries listed. The Saft battery is slightly smaller than standard D cells and may require bending of the battery clips for reliable contact.

All nickel-cadmium batteries exhibit the characteristic that, after several cycles of partial discharge followed by full recharging, there is a significant decrease in capacity. This may be corrected by allowing the batteries to fully discharge, then recharging them.

7.2 POWER DISTRIBUTION ASSEMBLY CHECKOUT AND REPAIR

The most common problems associated with the power distribution assembly are related to improper contact between the batteries and clips or between the voltage adapter output plug and connector JC1. See Fig. 7-1.

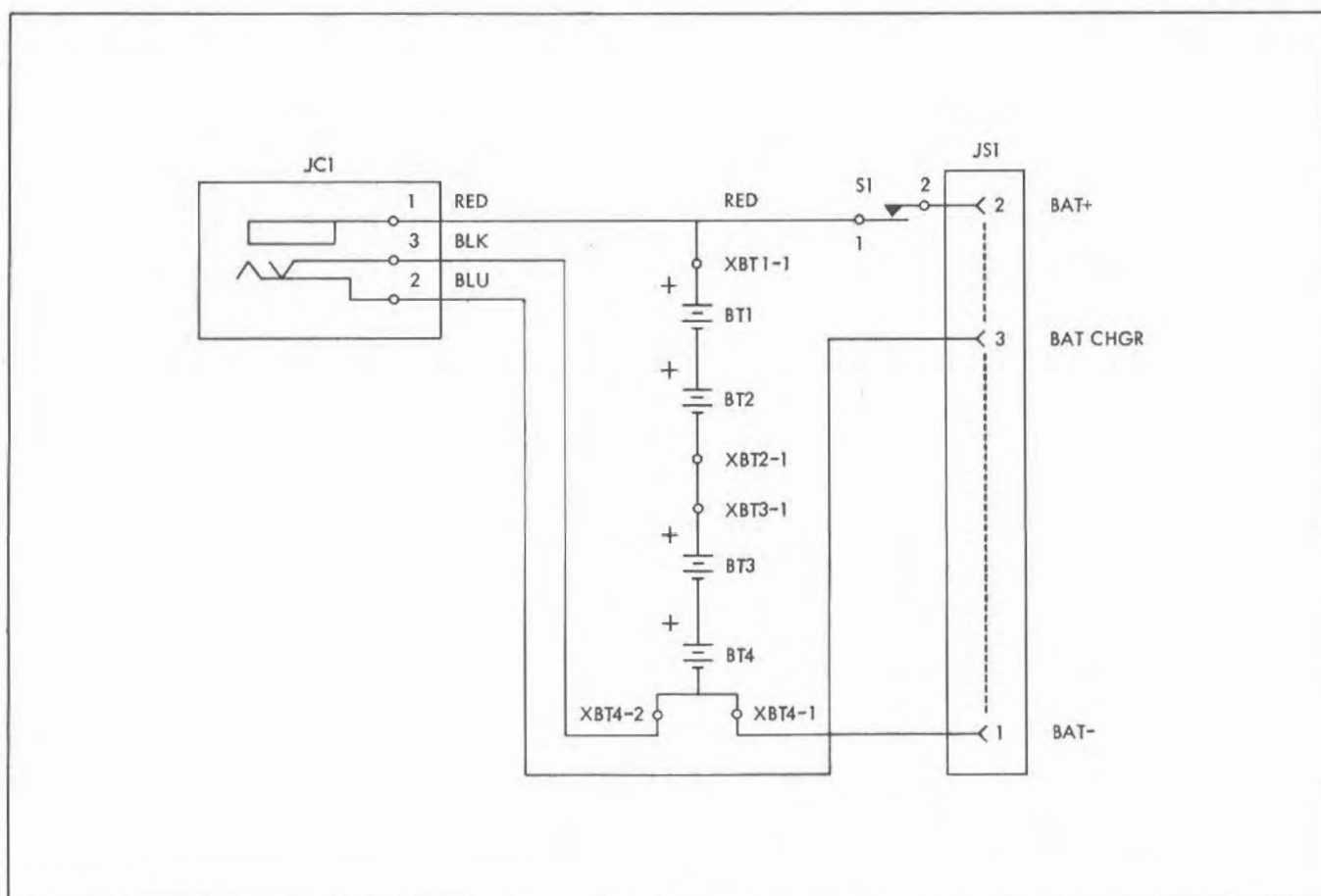


Fig. 7-1 Power Distribution Assembly Schematic Diagram

If the computer will operate on battery power but not from a good voltage adapter, reform the spring contact on JCI so it exerts greater pressure on the adapter plug, or replace the connector.

Excessive charging current with the computer turned off is usually caused by the connection between contacts 2 and 3 of JCI failing to open when the adapter is connected. To correct this, reform the spring contact of JCI so the adapter plug will break the connection when inserted. The batteries should be rechecked after this problem is corrected.

If the computer operates from the voltage adapter but not from good batteries, check the electrical contact of battery clips XBT1, XBT2, XBT3 and XBT4 with the batteries. If necessary, bend the clips to ensure reliable contact.

The battery clips with the insulated polarizing contacts should have the battery retainers clipped flush to the surface of the door. The clips with dimple contacts should be insulated with polyester-film, glass-filament tape.

7.3 CONVERTER BOARD TROUBLESHOOTING AND REPAIR

To troubleshoot the Converter board, install the defective board on an extender board in an otherwise properly operating computer and check the output voltages. See the assembly drawing, Fig. 7-2, and the schematic diagram, Fig. 7-3, to determine the most convenient test points. Voltage levels, with reference to V_{SS} , should be:

$$GND: -5 \pm 0.25V$$

$$V_{DD}: -7.5 \pm 0.25V$$

$$V_{GG}: -15 \pm 0.50V$$

$$V_{BIAS}: -60 \pm 6V$$

$$V_{KK}: -120 \pm 12V$$

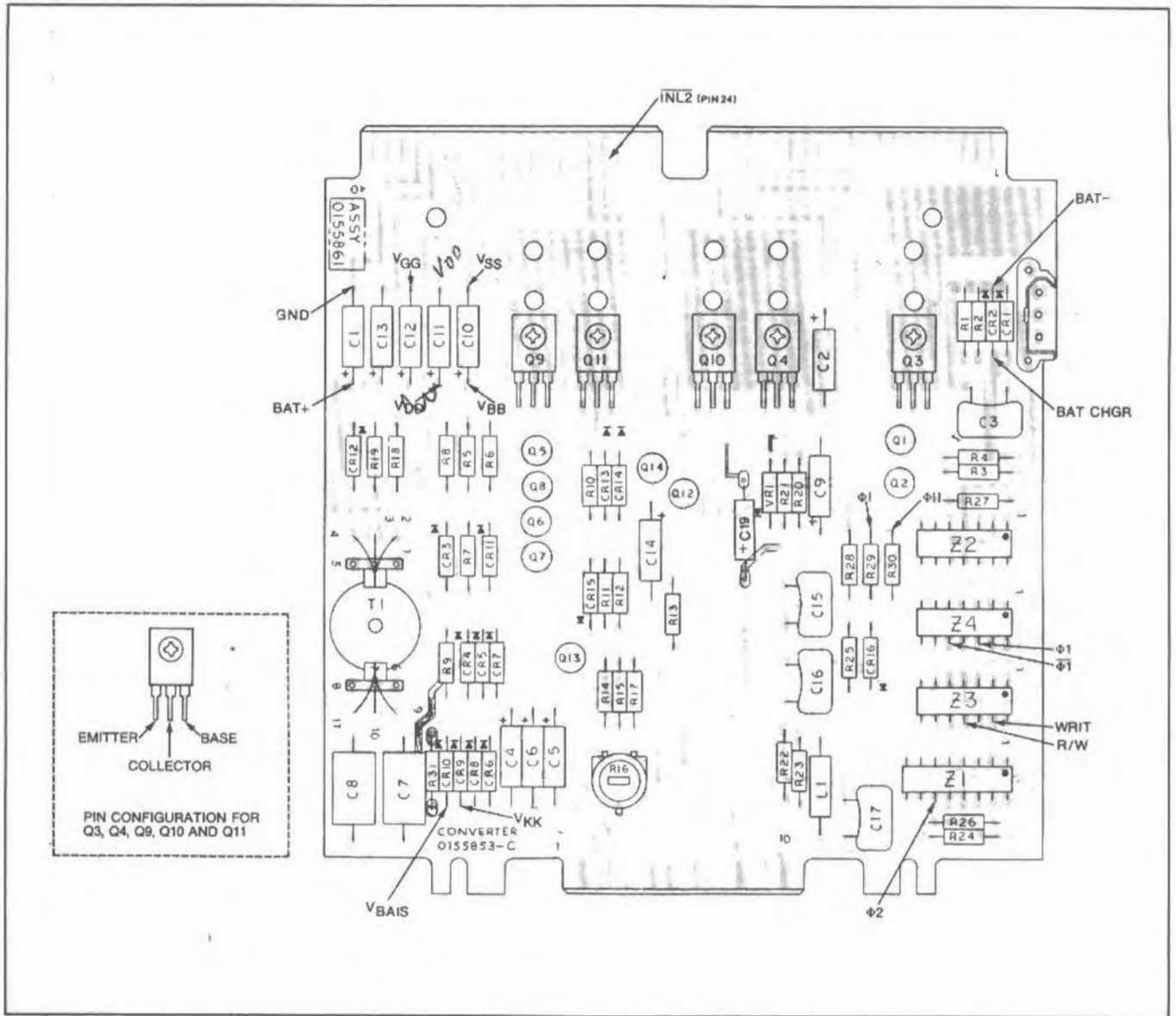


Fig. 7-2 Converter Board, Typical Test Points

The malfunction table, Table 7-2, lists the most probable causes of missing or incorrect voltages.

If all voltages except GND are completely missing, the clock circuit is probably inoperative.

If the computer draws more than 1.2 amperes from the adapter with the batteries removed, potentiometer R16 may require adjustment. If this symptom appears, adjust R16 so that VGG is exactly -15V and remeasure the current. If it still exceeds 1.2 amperes, the computer is defective.

Table 7-2

CONVERTER BOARD MALFUNCTION TABLE

Symptom	Possible Cause
Memory clears when adapter installed or disconnected	CR1, CR2
Excessive charging current	C3, CR1, CR2, Q1, Q2, Q3, R1, R2
Low or no charging current	C3, Q1, Q2, Q3, R1, R2, R3, R4
Premature low battery indication	C1, C14, R20, R31
No low battery indication	C1, C2, C14, Q14, R20, R21
Voltages will not adjust	C9, Q13, R13, R14, R15, R16, R17, VR1
V _{GG} low or missing	CR4, CR5, T1
V _{DD} low or missing	CR3, CR11, T1
GND missing	Q10, Q11, R12, T1
GND low	Q10, Q11, Q12, CR13, CR14, R11, T1, R12, Q13
GND low, all other voltages missing	Q4, Q5, Q6, Q7, Q8, Q9, T1, Clock Circuits
V _{BIAS} , V _{KK} low or missing	C4, C5, C6, C7, C8, CR6, CR7, CR8, CR9, CR10
Φ I, Φ II missing	R29, R30, Z2, Z4
Φ I missing	C18, R27, Z3, Z4
Φ R missing	R28, Z3, Z4
Φ I, Φ 2, Φ R missing	Z1
No clocks	C15, C16, L1, R22, R23, Z1, Z3

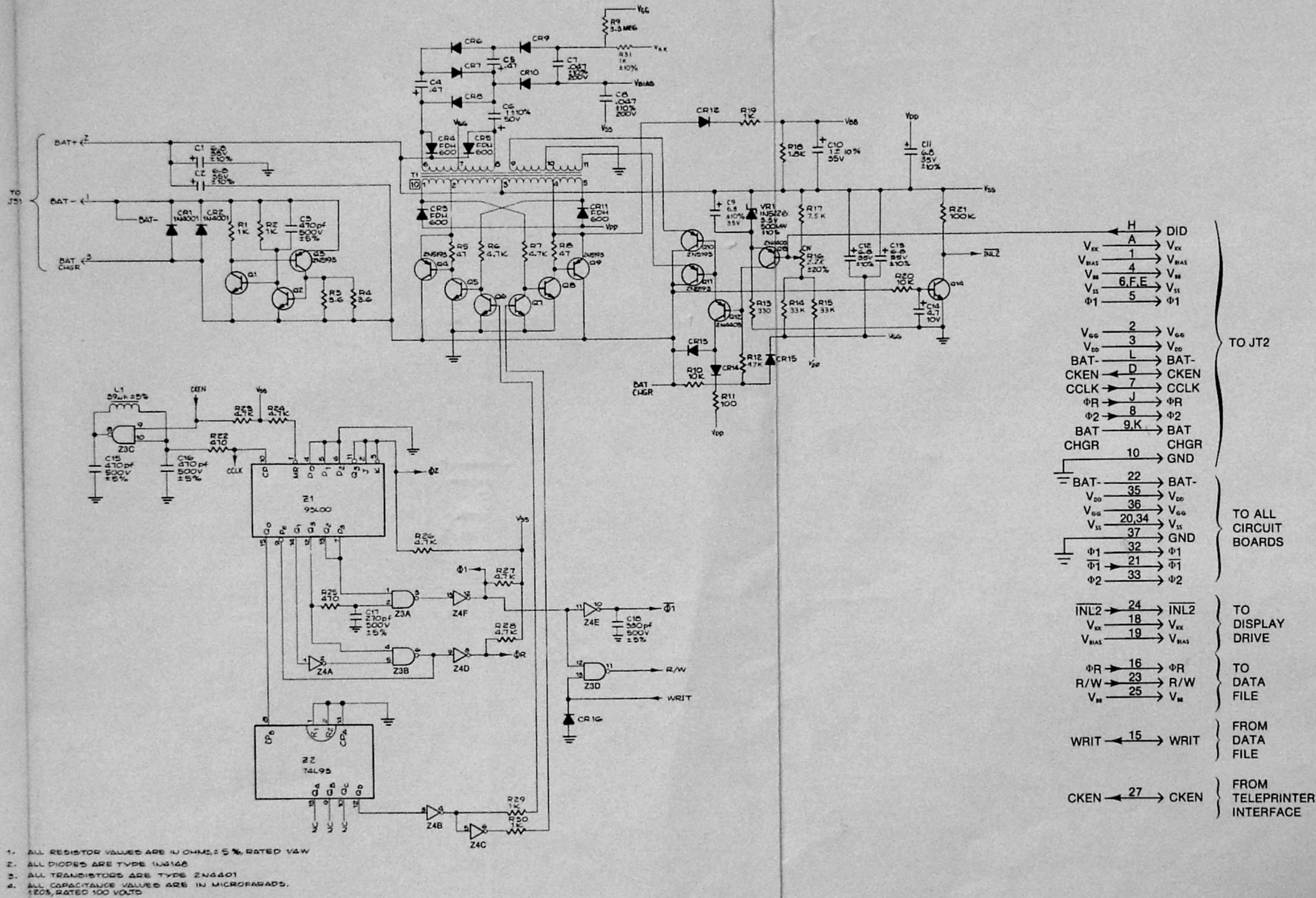


Fig. 7-3 Converter Board, Schematic Diagram

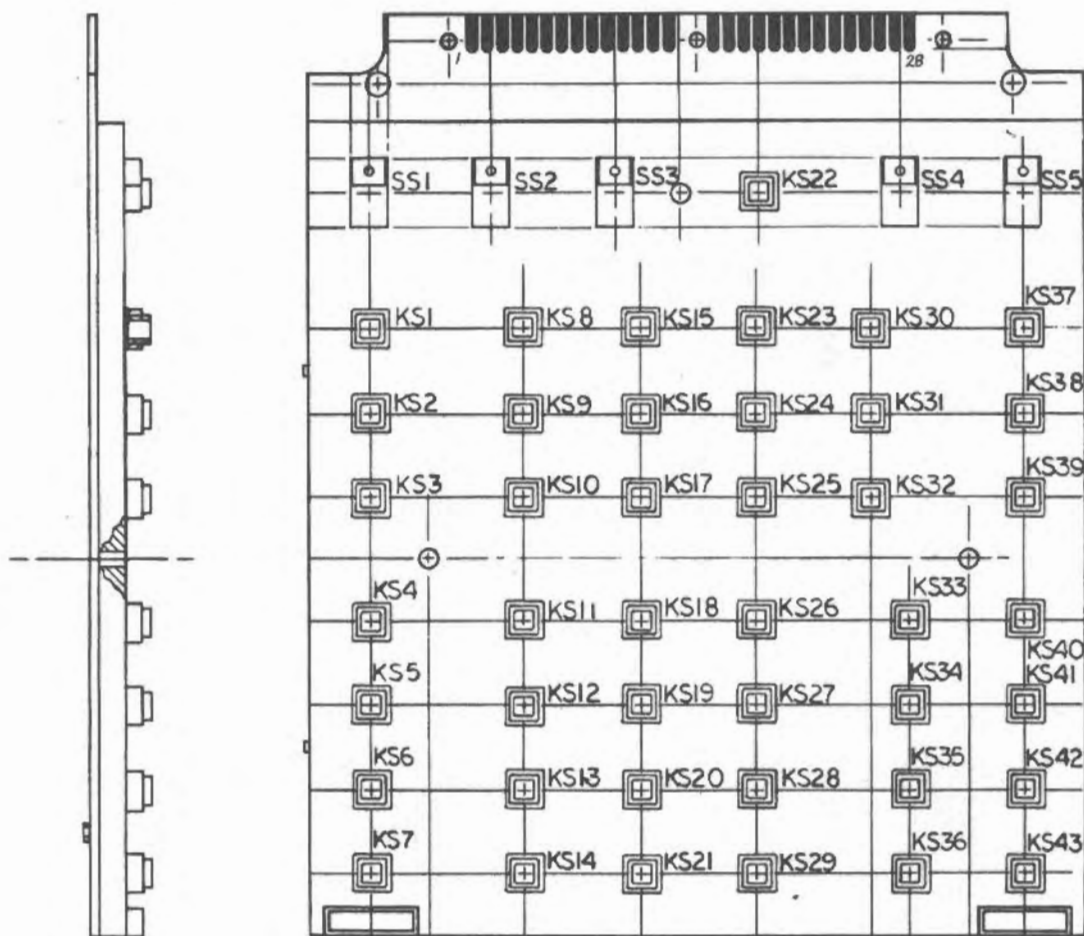


Fig. 8-2 Keyboard Assembly

Section VIII KEYBOARD CHECKOUT AND REPAIR

The keyboard construction is such that electrical failure, unless caused by contamination or physical damage, is very improbable. Therefore, this section primarily deals with symptoms of various mechanical problems.

8.1 INTERMITTENT SWITCHES

Intermittent operation of a key or slide switch may be caused by contaminated contacts. To remove foreign material, disassemble the keyboard as described in Par. 4.3. Clean the printed circuit card, slide switch contacts and domes with circuit board cleaner. Remove any corrosion with an ink or typewriter eraser.

A damaged keyboard cable may also cause intermittent operation.

8.2 DOMES FAILURES

If the keyboard causes the computer to lock up, go into Error or results in multiple entries, a dome is probably defective.

If a particular key switch causes one of the symptoms mentioned above, disassemble the keyboard as described in Par. 4.3 and replace the dome for that switch.

A dome may fail to return to its original shape after the key is released, and cause the computer to lock up. This defect may be tested with an ohmmeter; it will appear as a short between a Y line and a KX line. Determine the switch position from the schematic diagram, Fig. 8-1, and the assembly drawing, Fig. 8-2.

8.3 CABLE AND CIRCUIT CARD FAILURES

Neither the keyboard cable nor the printed circuit card is repairable, and should be replaced if defective.

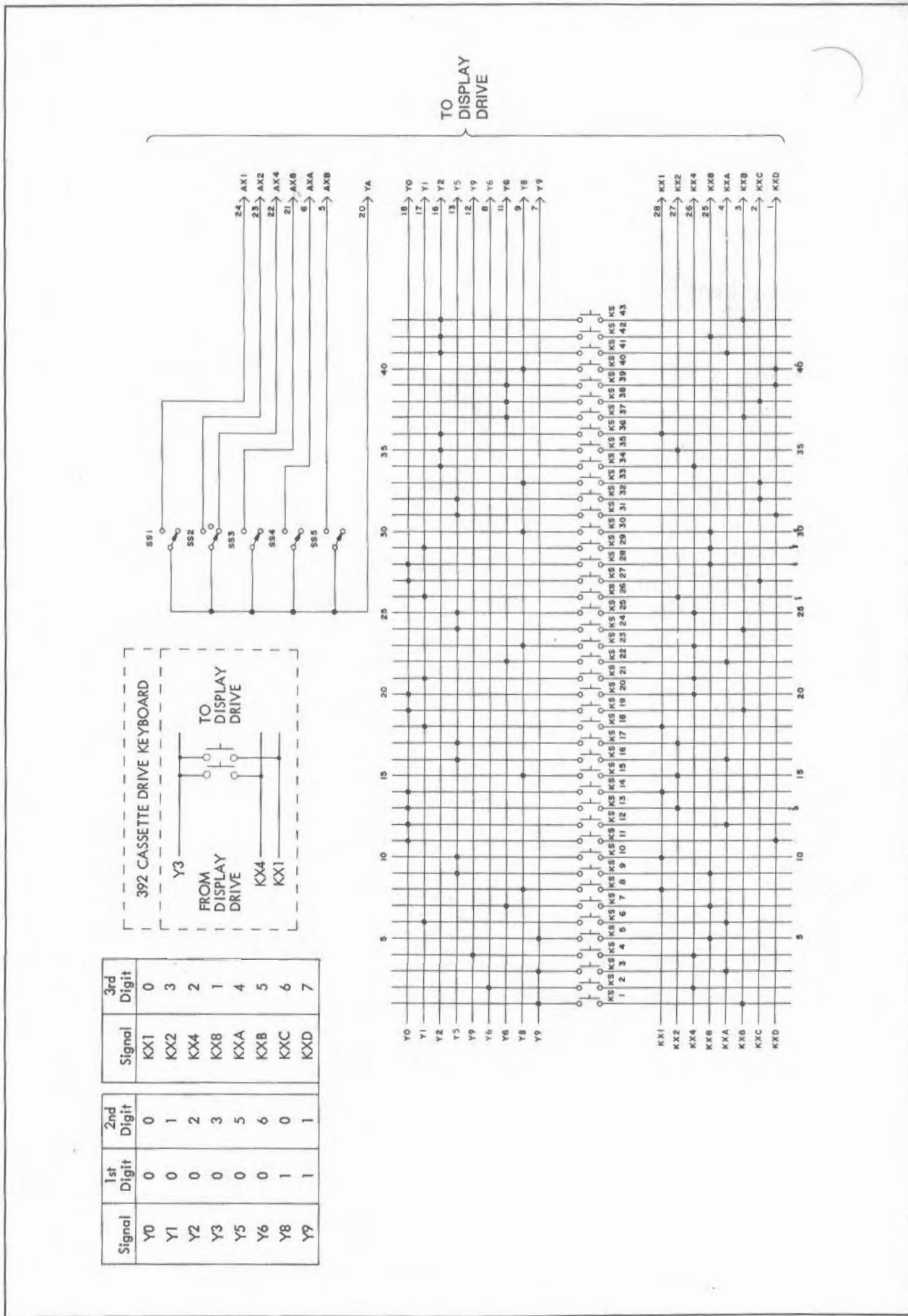


Fig. 8-1 Keyboard, Schematic Diagram

Section IX DISPLAY DRIVE AND DISPLAY CHECKOUT AND REPAIR

Section IX contains guides for testing and troubleshooting the Display Drive board and the display and display interconnect assemblies.

9.1 DISPLAY DRIVE CHECKOUT AND REPAIR

The Display Drive may be tested by executing the test procedure of Section III Table 3-1. Observe the test results for correct entry and the correct display.

The display control circuits, as well as the display itself, may be tested on the computer by executing the Self-Test procedure which is included in Table 3-1. The Self-Test program displays all segments of each digit position and the ROM and RAM check sums.

Refer to Figs. 9-1 through 9-3 for troubleshooting the Display Drive board.

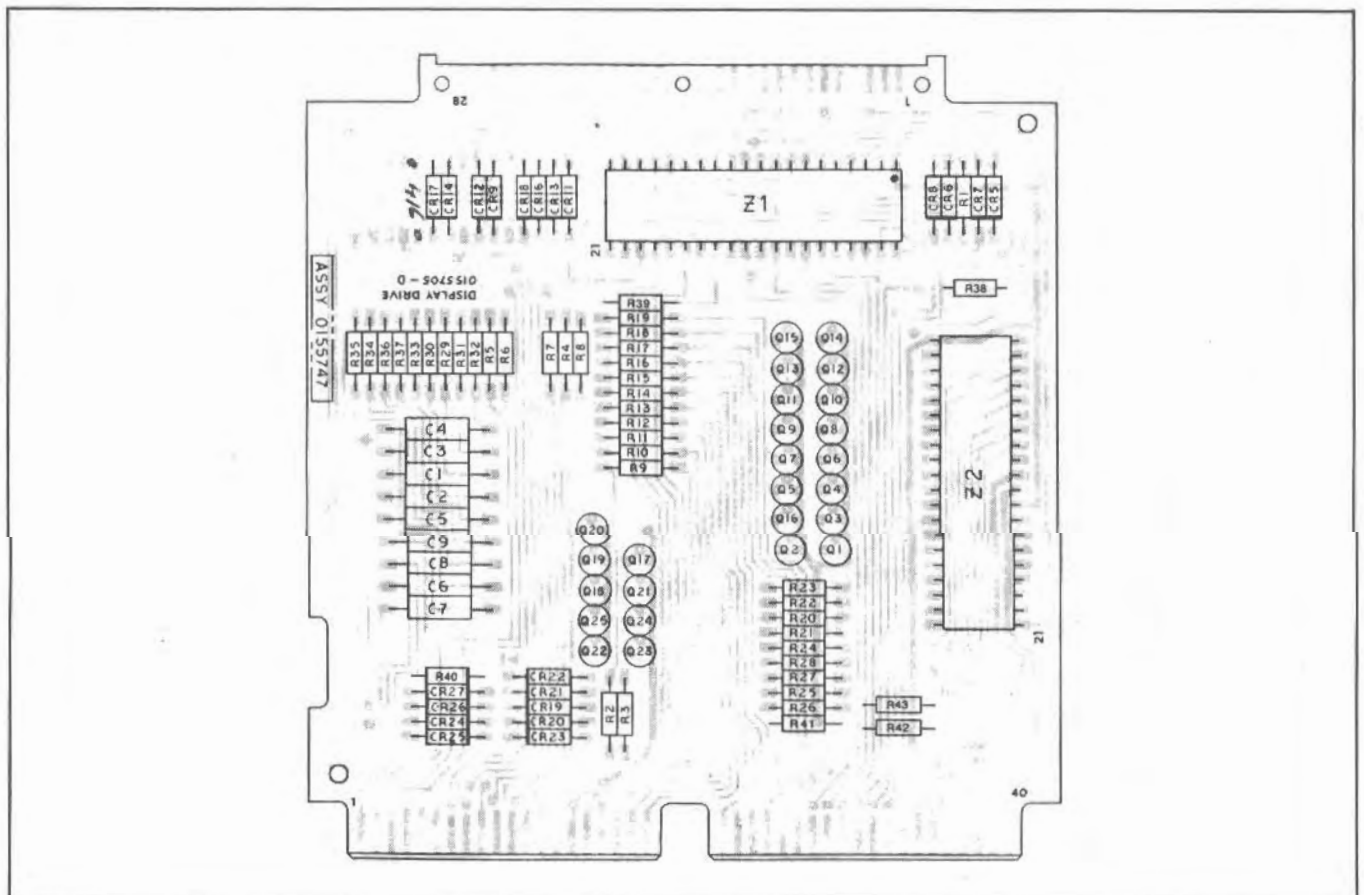


Fig. 9-1 Display Drive Board

9.1.1 INCORRECT DISPLAY

A display control malfunction may manifest itself by affecting a single display segment, a single digit position, or the entire display.

When a display malfunction is detected, first check the following Display Drive voltages.

GND: $-5 \pm 0.25V$

V_{KK} : $-120 \pm 12V$

V_{BIAS} : $-60 \pm 6V$

V_{DD} : $-7.5 \pm 0.25V$

V_{GG} : $-15.0 \pm 0.5V$

The voltages are measured with respect to V_{SS} .

When a particular segment is incorrect in all digit positions, refer to Table 9-1 for the probable component failure. Similarly, if a particular digit position displays incorrectly, refer to Table 9-2 for the probable cause. The anode positions are numbered from right to left. Figure 9-5 shows the segment configurations.

If these procedures do not identify the defective component, and the display and display interconnect assemblies are good, the ACL-08/TCL-08 should be replaced.

9.1.2 INCORRECT ENTRY

When an input error has been detected and isolated to the Display Drive board, verify that all Display Drive voltages are correct. Next, check the isolation diodes CR5 through CR9, and CR11 through CR14 with an ohmmeter. If a diode is not the cause of the malfunction, replace the keyscanner chip (ACL-02/TCL-02).

Table 9-1
SEGMENT DRIVE COMPONENTS

Segment	Cathode Transistor	Base Limiting Resistor	Coupling Circuit			Segment Symptoms				
						Always Off				All Segments Off
a.	Q25	R28	C9	CR27	R37	Q25	R28	C9	CR27	R37
b.	Q24	R27	C8	CR26	R36	Q24	R27	C8	CR26	R36
c.	Q23	R26	C7	CR25	R35	Q23	R26	C7	CR25	R35
d.	Q18	R21	C2	CR20	R30	Q18	R21	C2	CR20	R30
e.	Q17	R20	C1	CR19	R29	Q17	R20	C1	CR19	R29
f.	Q20	R23	C4	CR22	R32	Q20	R23	C4	CR22	R32
g.	Q19	R22	C3	CR21	R31	Q19	R22	C3	CR21	R31
DP	Q22	R25	C6	CR24	R34	Q22	R25	C6	CR24	R34
Comma	Q21	R24	C5	CR23	R33	Q21	R24	C5	CR23	R33

9.2 DISPLAY AND DISPLAY INTERCONNECT MALFUNCTION

When either the display or interconnect assembly is suspected of malfunction, first check that the display is properly aligned on the interconnect, no interconnect leads are shorted together and that the interconnect board is firmly mounted in the terminal block.

Figure 9-4, Display Interconnect Assembly, and Fig. 9-6, Display Interconnect Schematic Diagram, are included for reference.

The display assembly is not repairable. If substitution verifies that the display is defective, the display should be replaced.

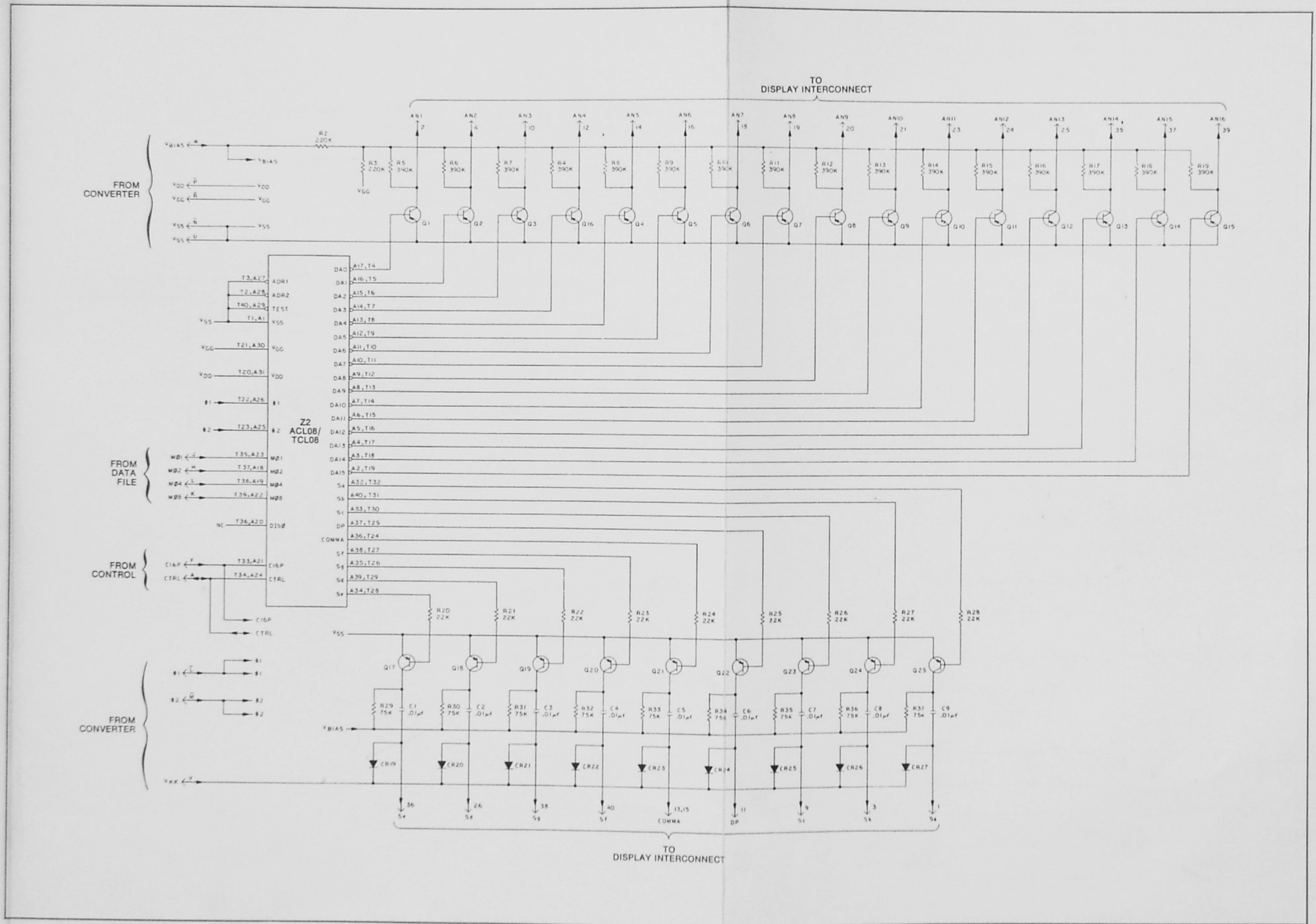


Fig. 9-2 Display Control Schematic Diagram

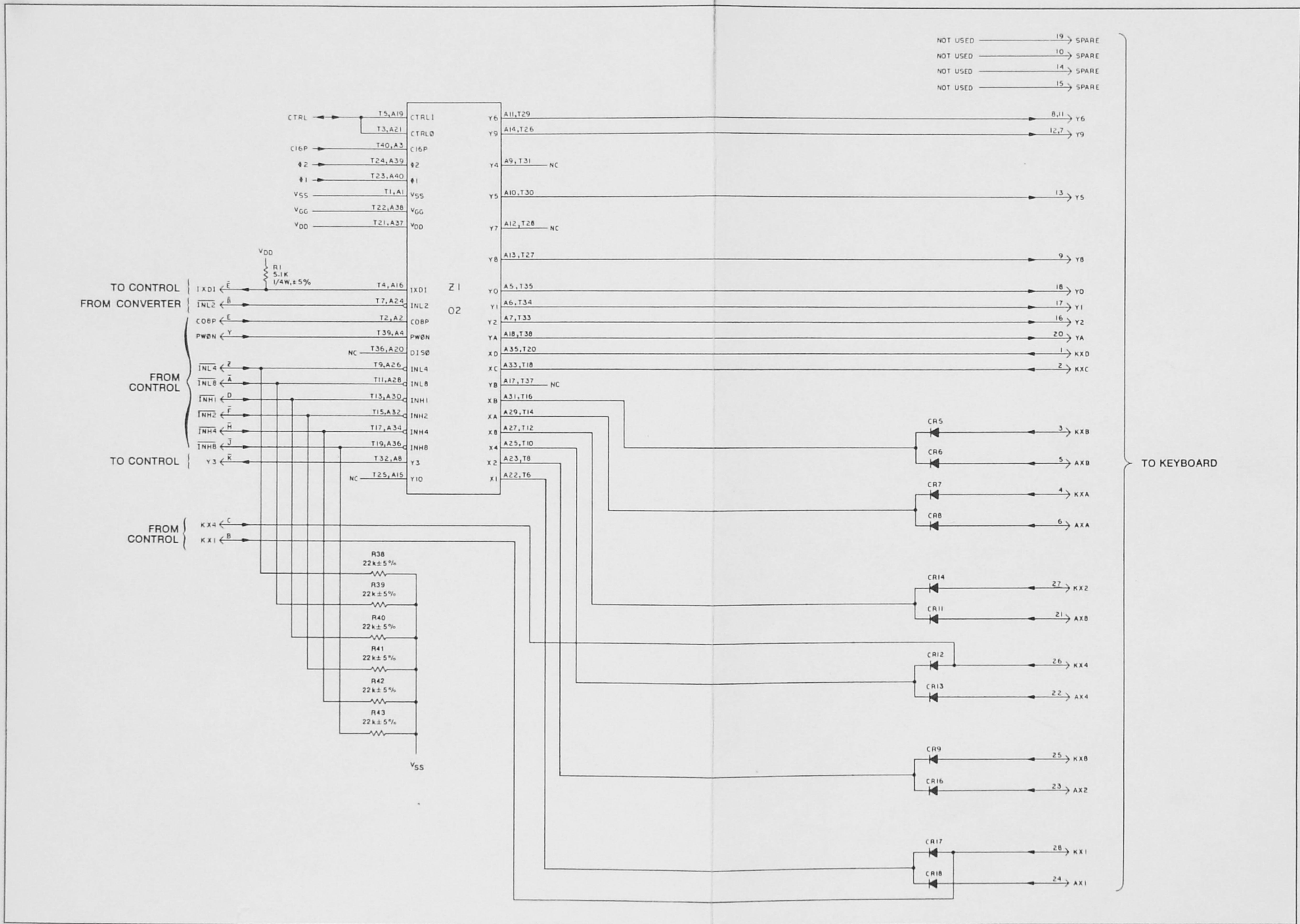


Fig. 9-3 Keyscanner Circuits, Typical Schematic Diagram

Table 9-2
ANODE DRIVE COMPONENTS

Position	Transistor	Resistor	Digit		
			Always On	Always Off	Intermittent
1	Q1	R5	Q1 is shorted	Q1 is open	R5 is open
2	Q2	R6	Q2 is shorted	Q2 is open	R6 is open
3	Q3	R7	Q3 is shorted	Q3 is open	R7 is open
4	Q16	R4	Q16 is shorted	Q16 is open	R4 is open
5	Q4	R8	Q4 is shorted	Q4 is open	R9 is open
6	Q5	R9	Q5 is shorted	Q5 is open	R9 is open
7	Q6	R10	Q6 is shorted	Q6 is open	R10 is open
8	Q7	R11	Q7 is shorted	Q7 is open	R11 is open
9	Q8	R12	Q8 is shorted	Q8 is open	R12 is open
10	Q9	R13	Q9 is shorted	Q9 is open	R13 is open
11	Q10	R14	Q10 is shorted	Q10 is open	R14 is open
12	Q11	R15	Q11 is shorted	Q11 is open	R15 is open
13	Q12	R16	Q12 is shorted	Q12 is open	R16 is open
14	Q13	R17	Q13 is shorted	Q13 is open	R17 is open
15	Q14	R18	Q14 is shorted	Q14 is open	R18 is open
16	Q15	R19	Q15 is shorted	Q15 is open	R19 is open

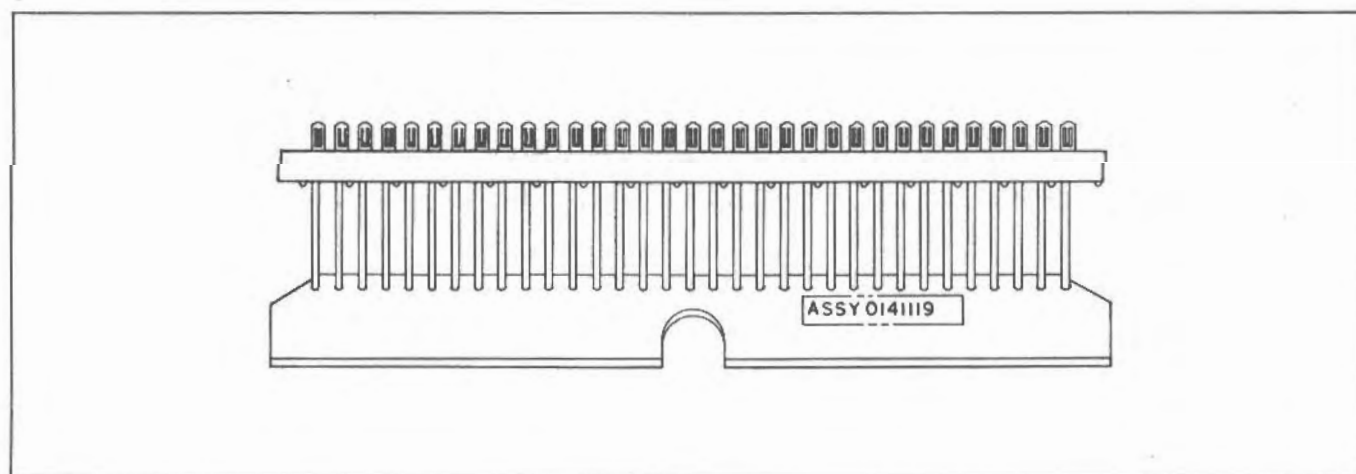


Fig. 9-4 Display Interconnect Assembly

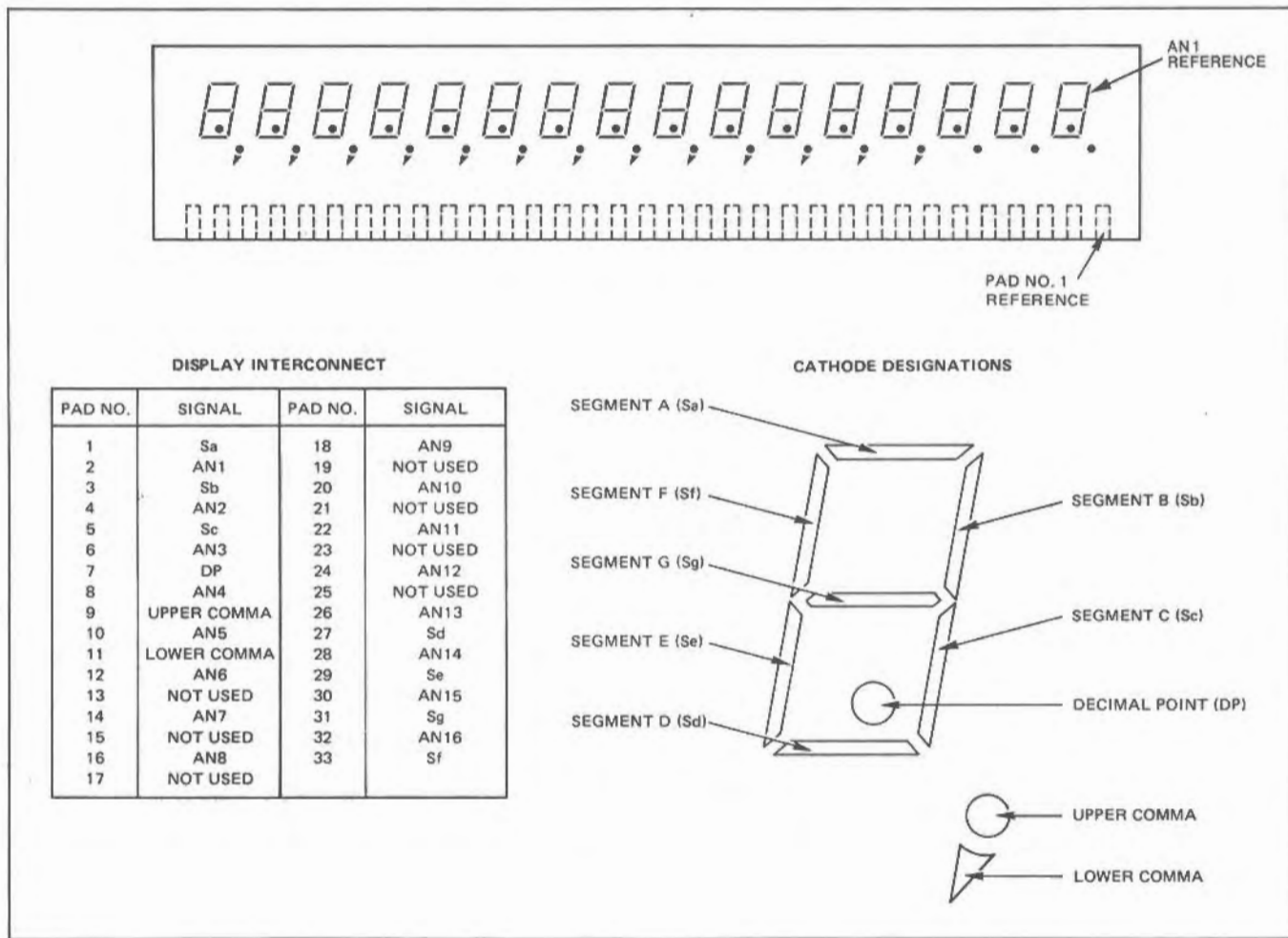


Fig. 9-5 Panaplex II Display Assembly

01-6

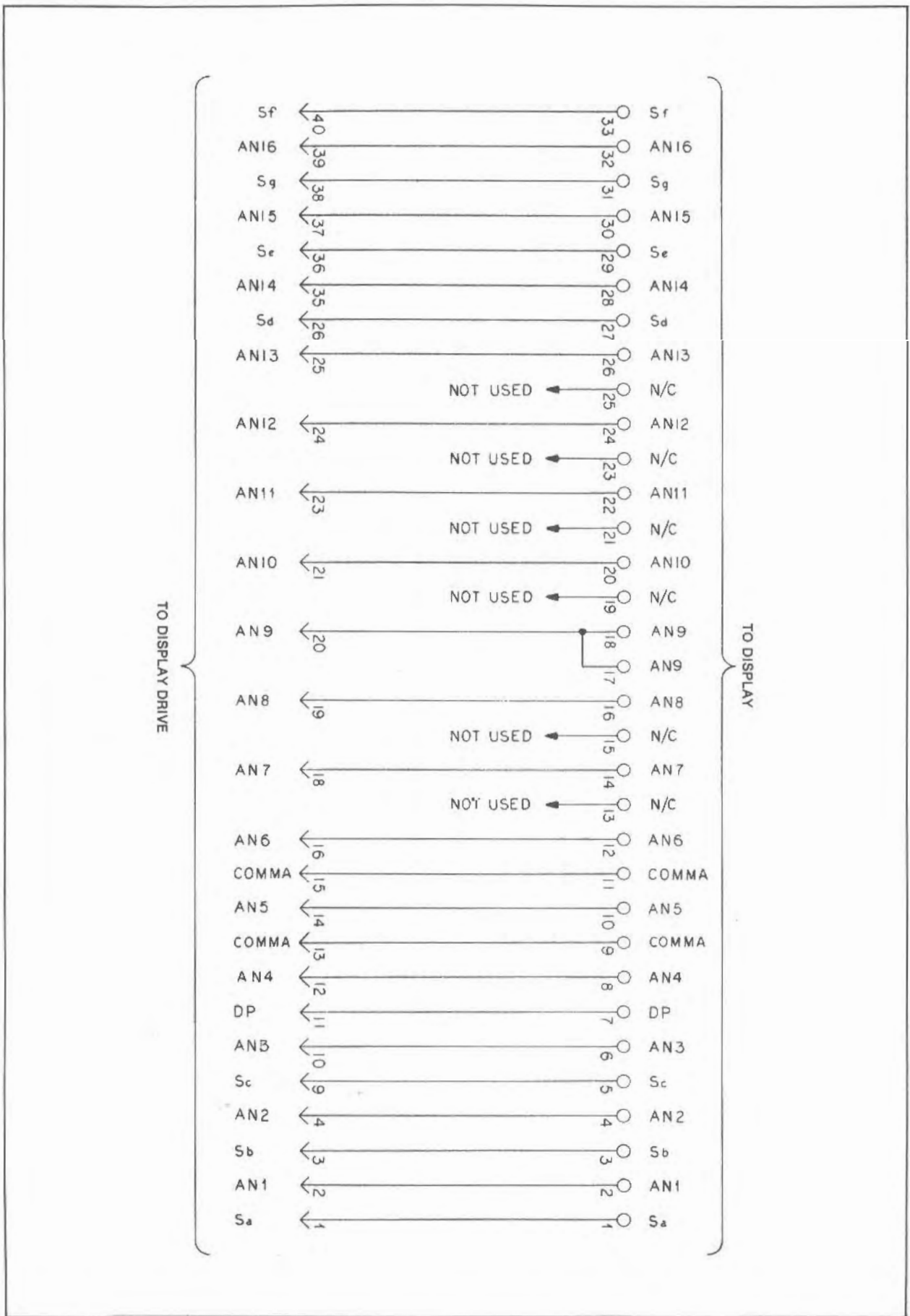


Fig. 9-6 Display Interconnect Schematic Diagram